

54321

D

C

B

A

OSLO SKL-H

Schematics Document

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<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A

Document Number
OSLO-SKLH

Rev
SA

Date: Saturday, July 11, 2015

Sheet 1 of 105

54321

D

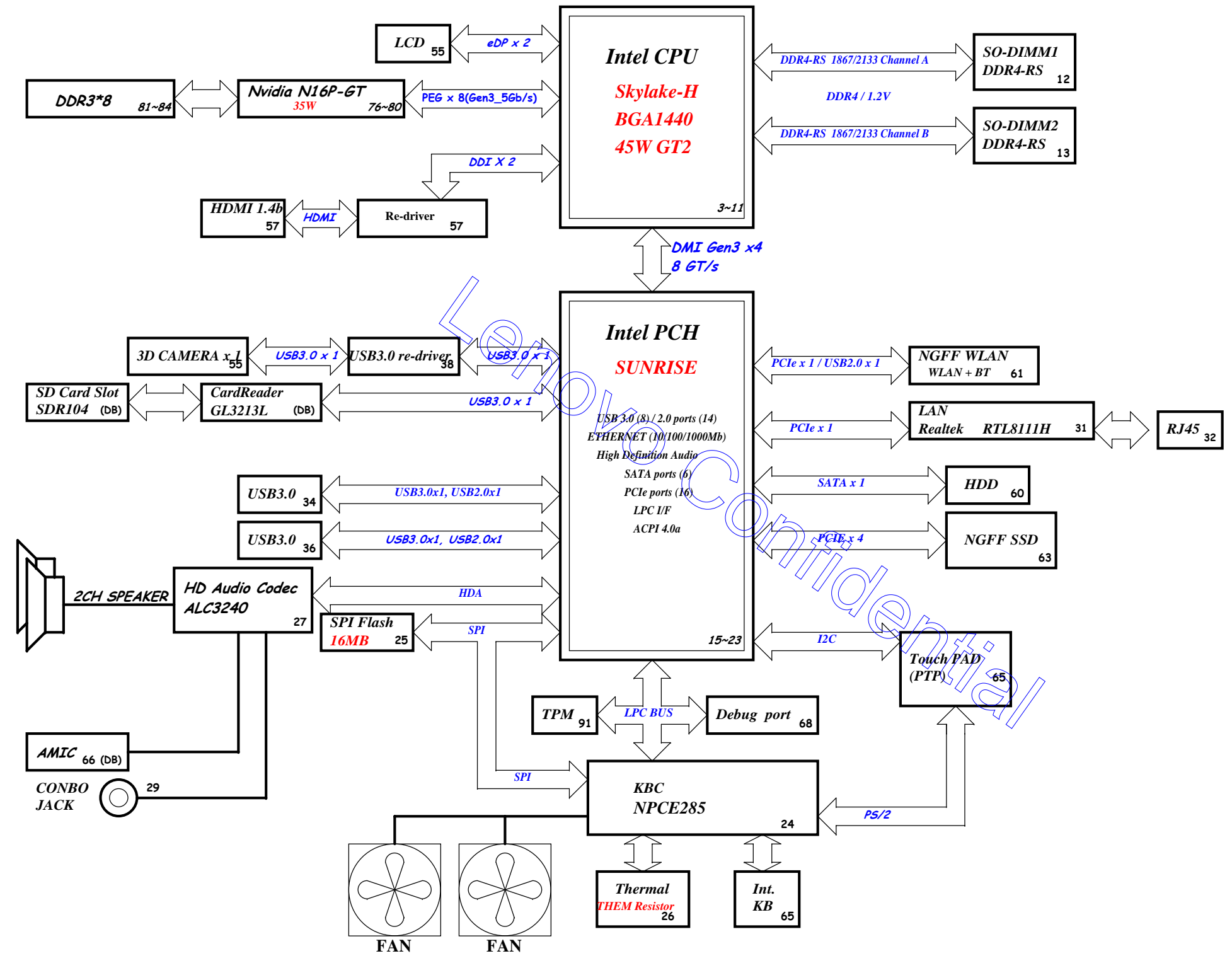
C

B

A

OSLO SKL-H Board Block Diagram

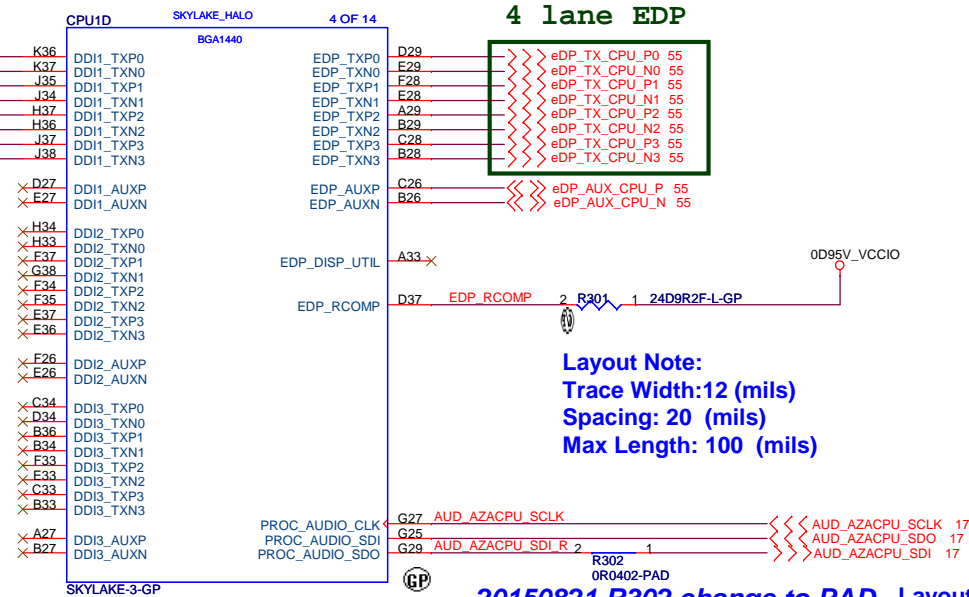
Project code : 4PD06R010001
PCB P/N : 15221
Revision : SA



SSID = CPU

57 HDMI_DATA2
57 HDMI_DATA2#
57 HDMI_DATA1#
57 HDMI_DATA1#
57 HDMI_DATA0#
57 HDMI_DATA0#
57 HDMI_CLK#
57 HDMI_CLK#

0512 wei



Layout Note:
Trace Width:12 (mils)
Spacing: 20 (mils)
Max Length: 100 (mils)

Layout Note:
Trace Width:12 (mils)
Spacing: 15 (mils)
Max Length: 400 (mils)



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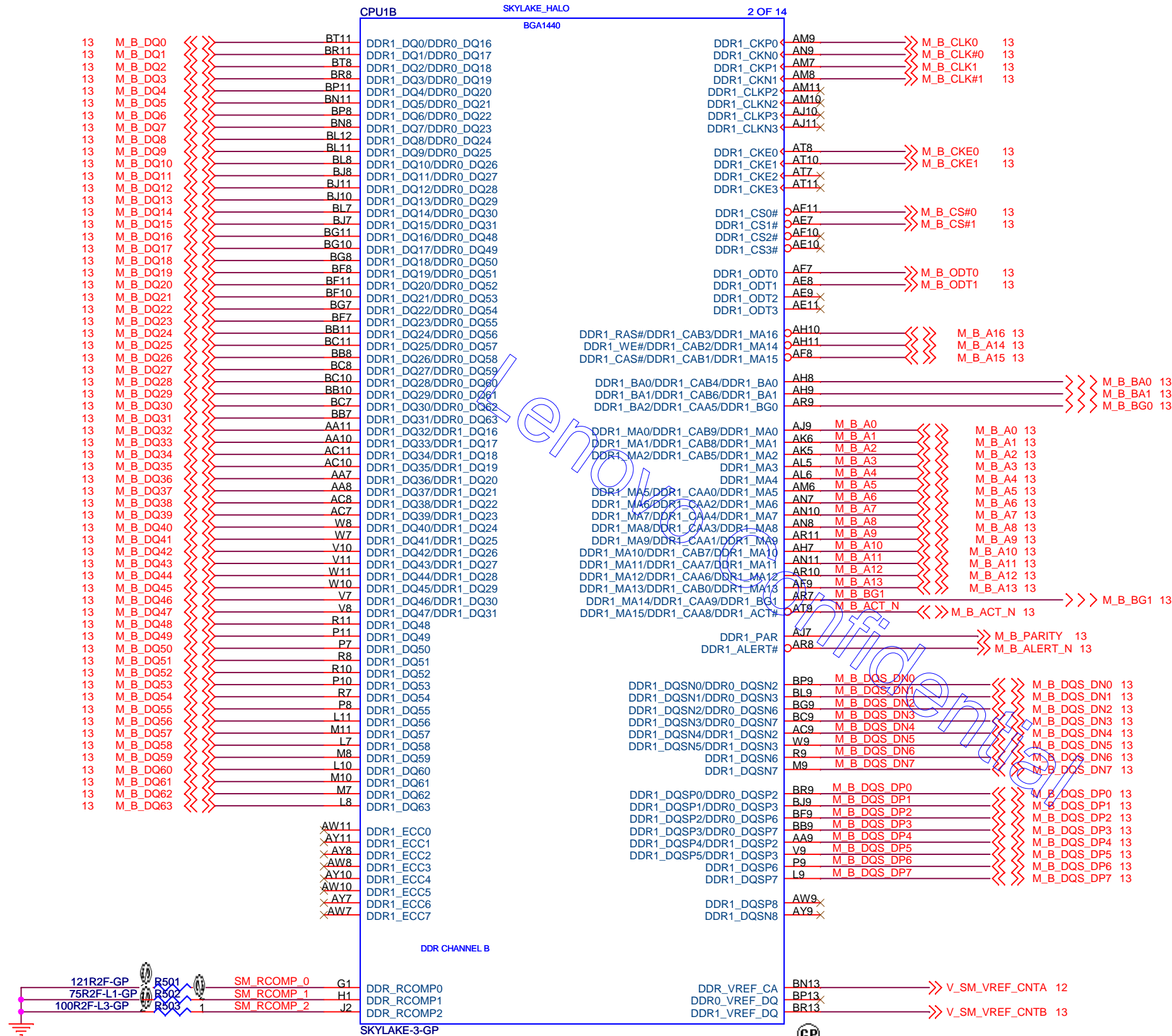
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Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (PCIe/DMI/FDI)

Size Custom Document Number Merlyn-SKLH Rev SC

Date: Friday, August 21, 2015 Sheet 3 of 105

SSID = CPU



CPU BOM CTRL

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Title

CPU DDR CHBSize
A3

Document Number

OSLO-SKLH

ev

SC

Date: Saturday, July 11, 2015

Sheet

of

05

SSID = CPU

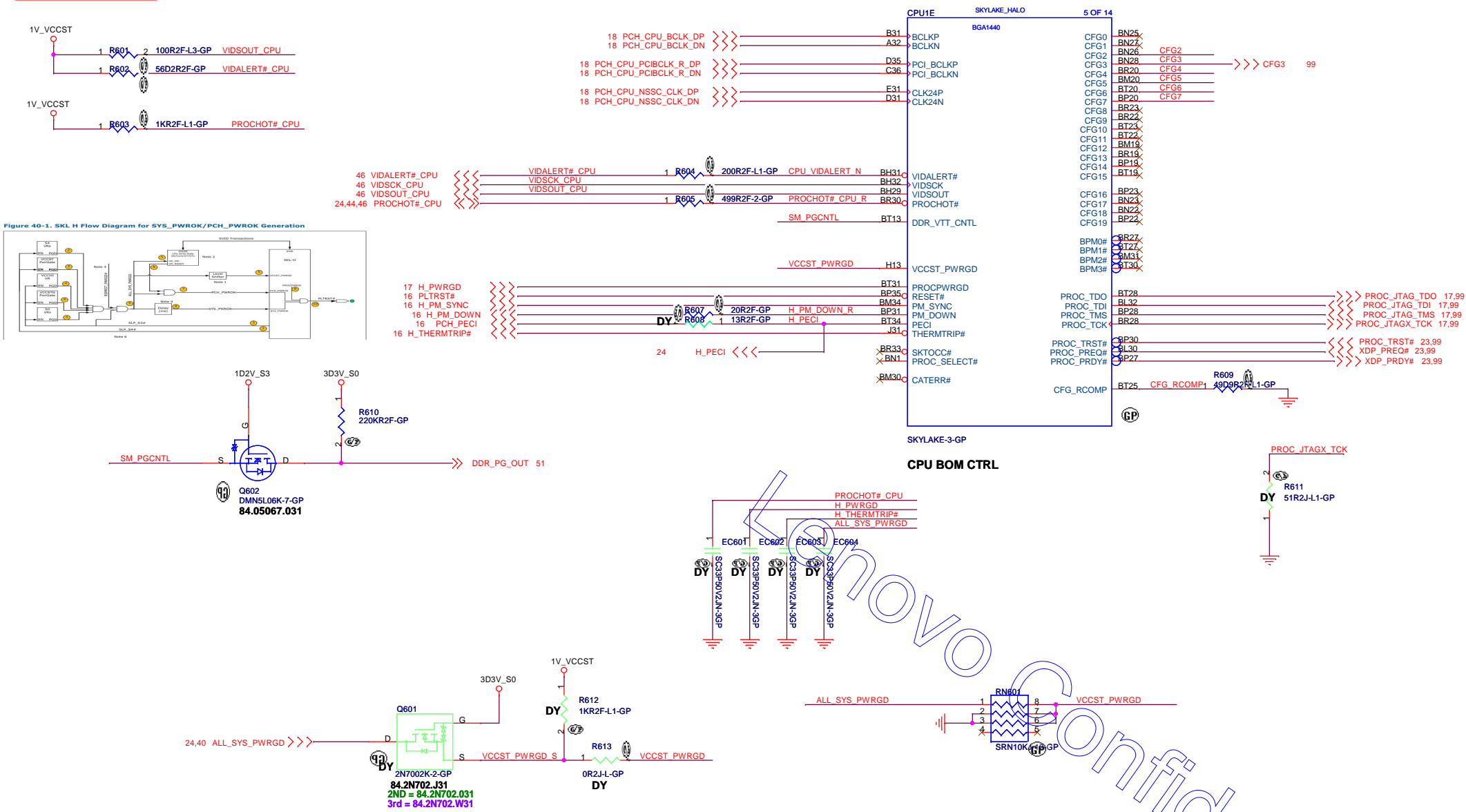


Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: <ul style="list-style-type: none"> 1 = (Default) Normal Operation; No stall. 0 = Stall. CFG[1]: Reserved configuration lane. CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> 1 = Normal operation 0 = Lane numbers reversed. CFG[3]: Reserved configuration lane. CFG[4]: eDP enable: <ul style="list-style-type: none"> 1 = Disabled. 0 = Enabled. CFG[6:5]: PCI Express* Bifurcation <ul style="list-style-type: none"> 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express* CFG[7]: PEG Training: <ul style="list-style-type: none"> 1 = (default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training. CFG[19:8]: Reserved configuration lanes. 	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

Processor Internal Pull-Up / Pull-Down Terminations

Processor Internal Pull-Up / Pull-Down Terminations

Signal Name	Pull Up/Pull Down	Rail	Value
BPM[3:0]	Pull Up	VCC _{IO}	16-60 Ω
PREQ#	Pull Up	VCC _{ST}	3 kΩ
PROC_TDI	Pull Up	VCC _{STG} ¹	3 kΩ
PROC_TMS	Pull Up	VCC _{SGT} ¹	3 kΩ
CFG[19:0]	Pull Up	VCC _{IO}	3 kΩ

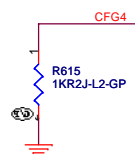
Note:

1. For SKL-S it should be VCC_{ST}

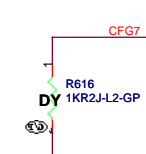
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



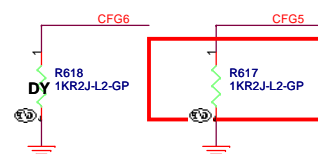
eDP Enable	
CFG4	1: Disable 0: Enable



PEG Training	
CFG7	1: (default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training.



PCIe Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved - (Device 1 function 1 disabled; function 2 enabled) 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

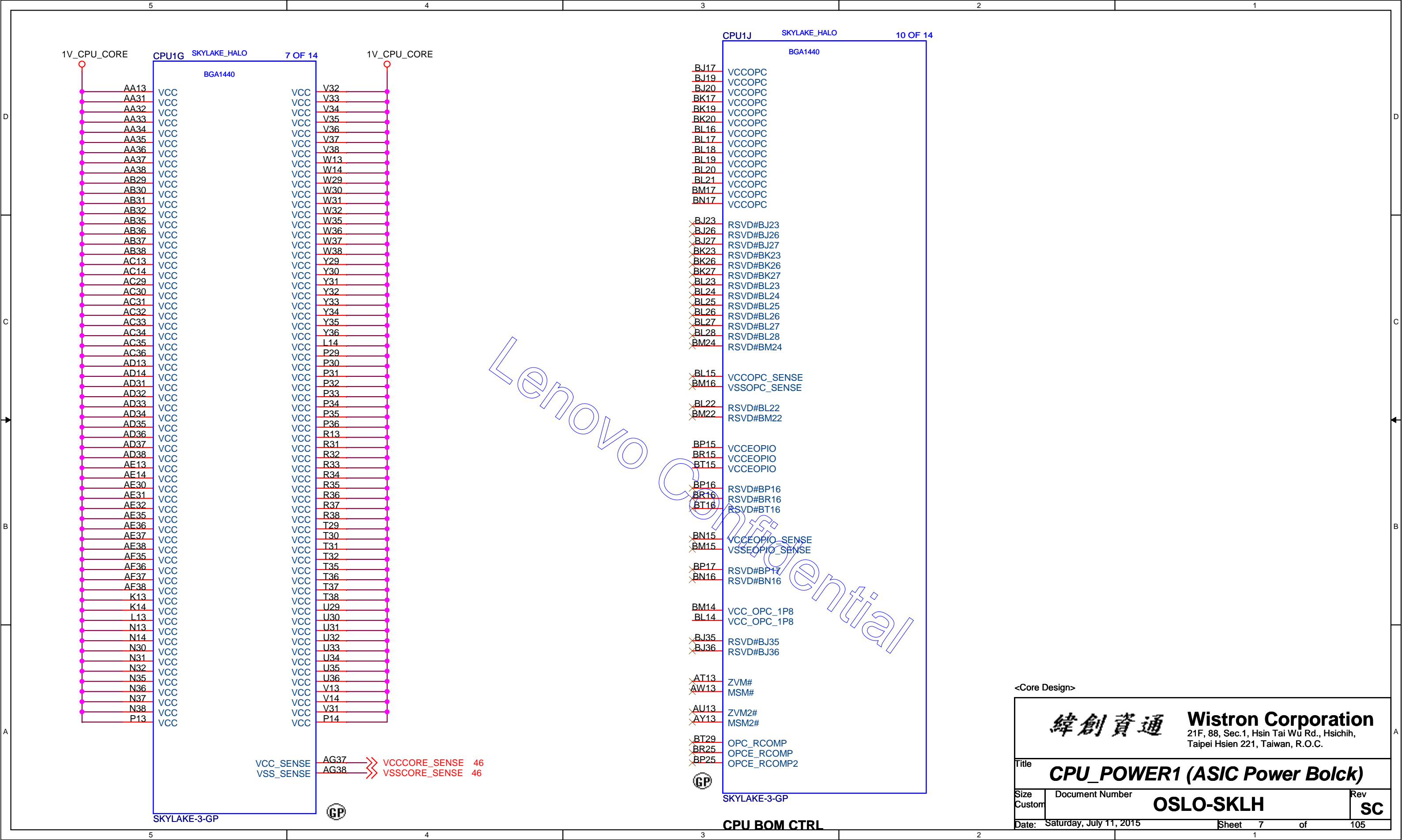


20150824 install R617

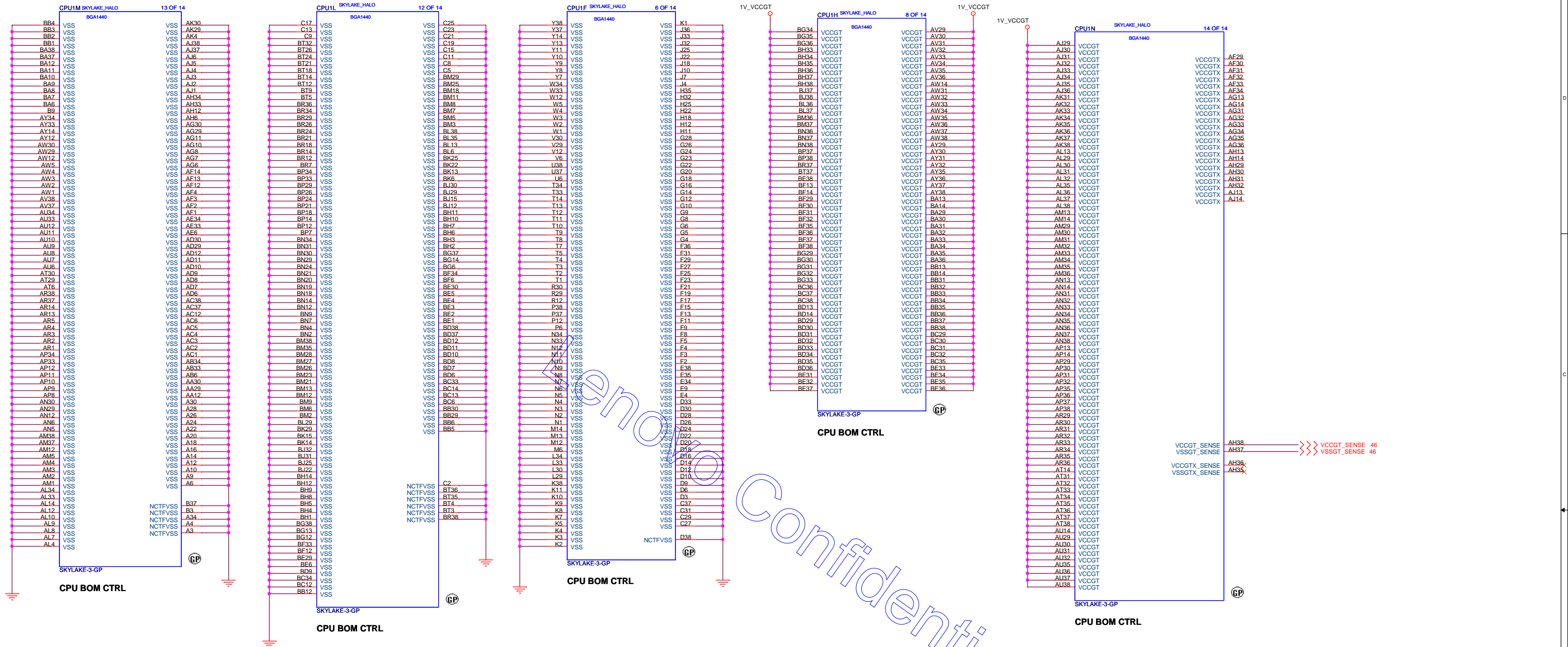
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Title			
CPU CFG CFG STRAP			
Size A2	Document Number	Rev	SC
OSLO-SKLH			
Date: Monday, August 24, 2015	Sheet 6	of	105

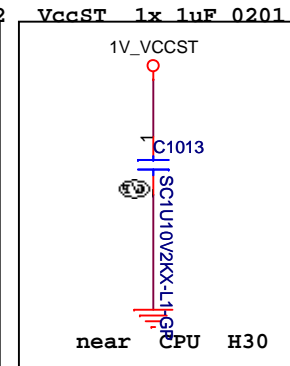
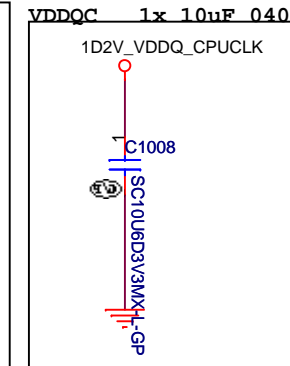
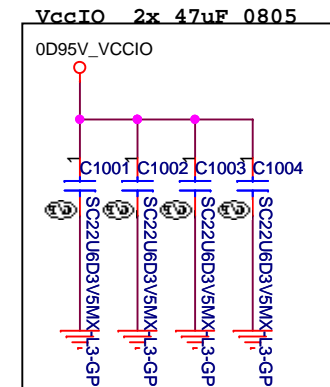
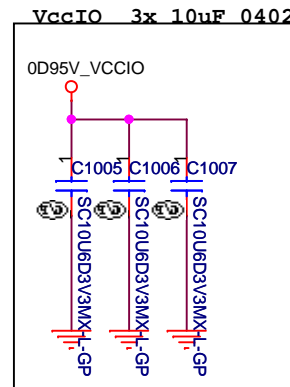
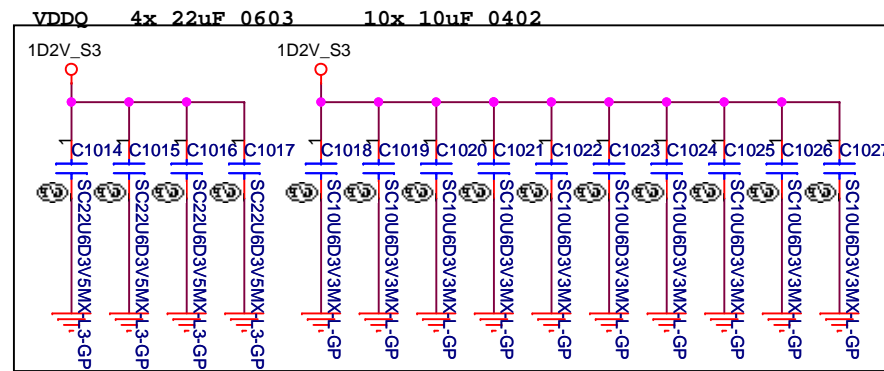
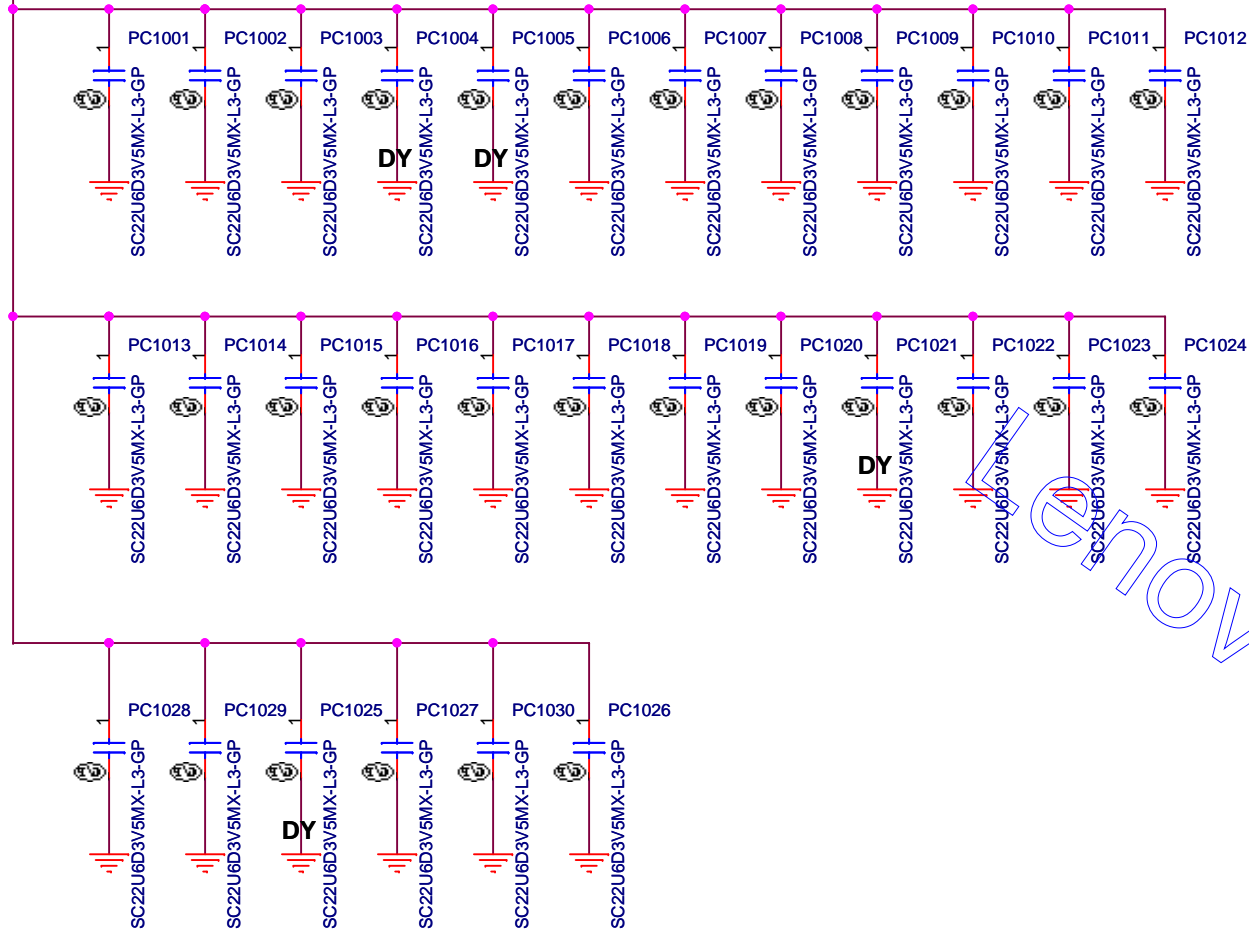


SSID = CPU

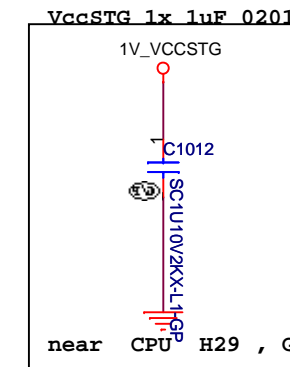
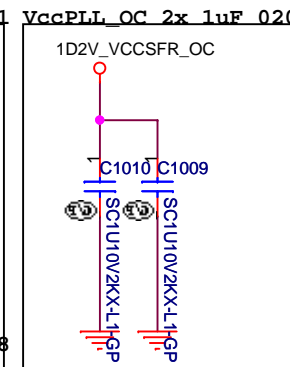
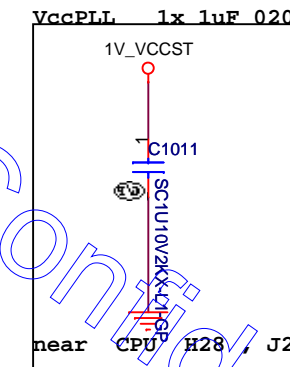


1V_CPU_CORE

20150923 DY PC1025, PC1004, PC1005, PC1021, for decap



VR: +/-5% or +/-50mV
Place close to VR output



JJ 20150130

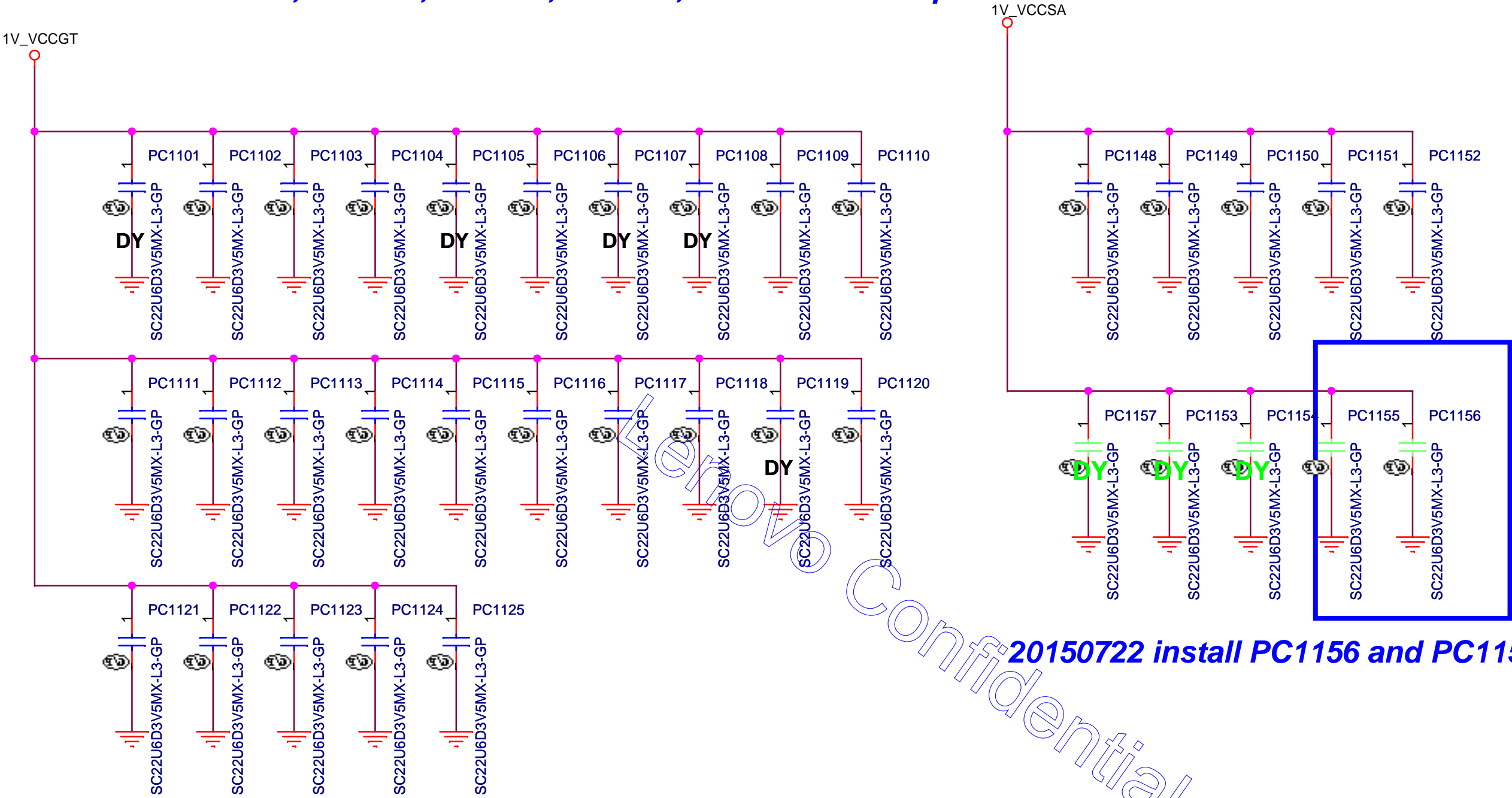
Decoupling Requirements for SKL H Processor (Sheet 2 of 2)

Domain	Board Edge cap	Backside cap	Notes
VCCGT	6x 47uF 0805		
		8x 22uF 0603	
		35x 10uF 0402	
		68x 1uF 0201	
VCCGTx	8x 22uF 0603		
		4x 10uF 0402	
VCCSA	1x 47uF 0805		
		1x 47uF 0805	
		7x 10uF 0402	
		3x 1uF 0201	
VDDQ		4x 22uF 0603	Share supply with DRAM
		10x 10uF 0402	
VDDQC		1x 10uF 0402	
VCCIO	2x 47uF 0805		VR: +/-5% or +/-50mV Place close to VR output
		3x 10uF 0402	
VCCST		1x 1uF 0201	
VCCSTG		1x 1uF 0201	Share supply with 1.0V PCH rail
VCCPLL		1x 1uF 0201	
VCCPLL_OC		2x 1uF 0201	Supply from 1.2V VDDQ
VCCOPC		10x 10uF 0402	VR: +/-5% or +/-50mV
VCCOPPG		3x 10uF 0402	VR: +/-5% or +/-50mV

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Title		
010_CPU (Power CAP1)		
Size A3	Document Number	Rev
	OSLO-SKLH	SC
Date: Wednesday, September 23, 2015	Sheet 10	of 105

20150923 DY PC1107, PC1108, PC1119, PC1101, PC1105 for decap

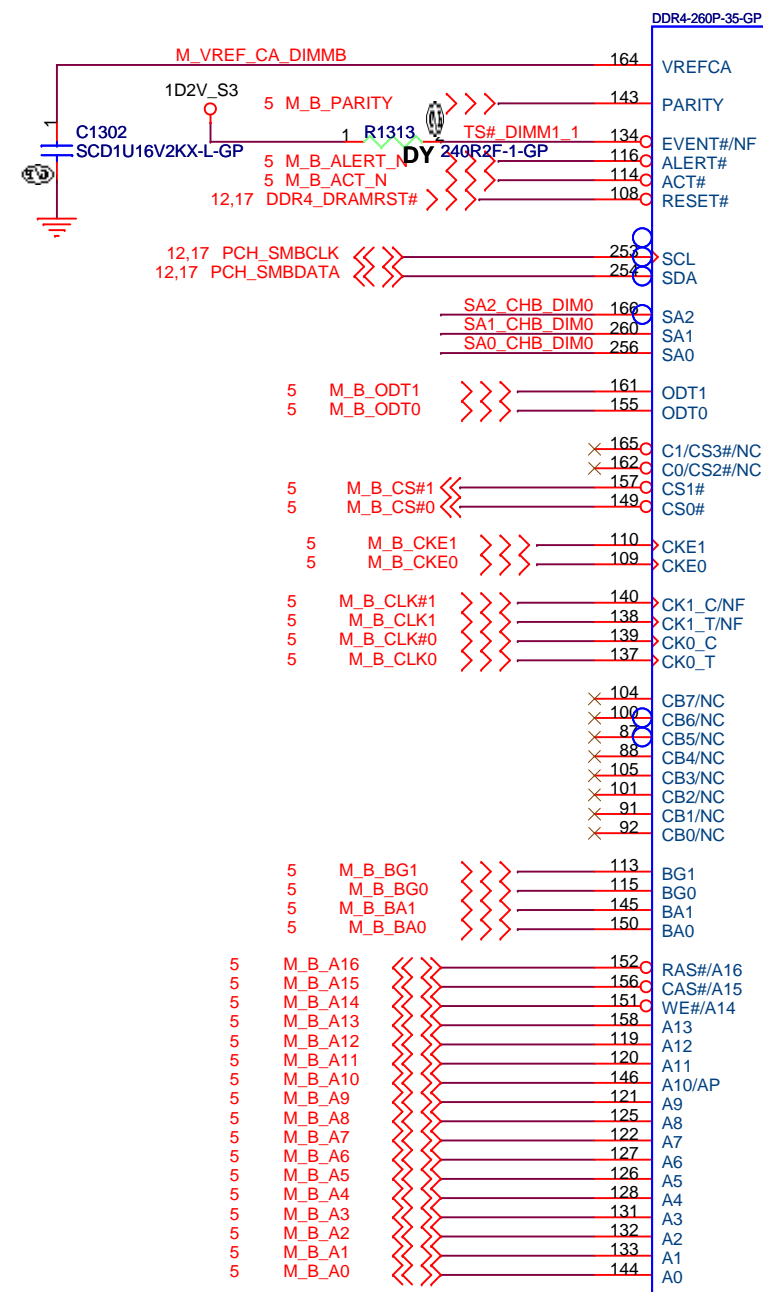


20150722 install PC1156 and PC1155 for power

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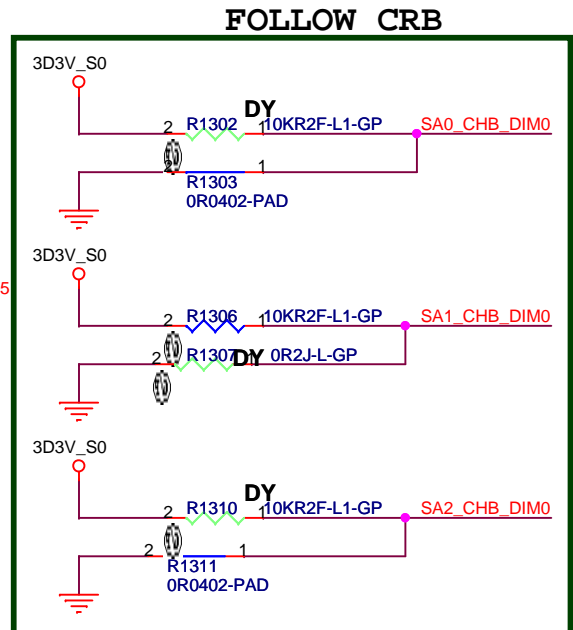
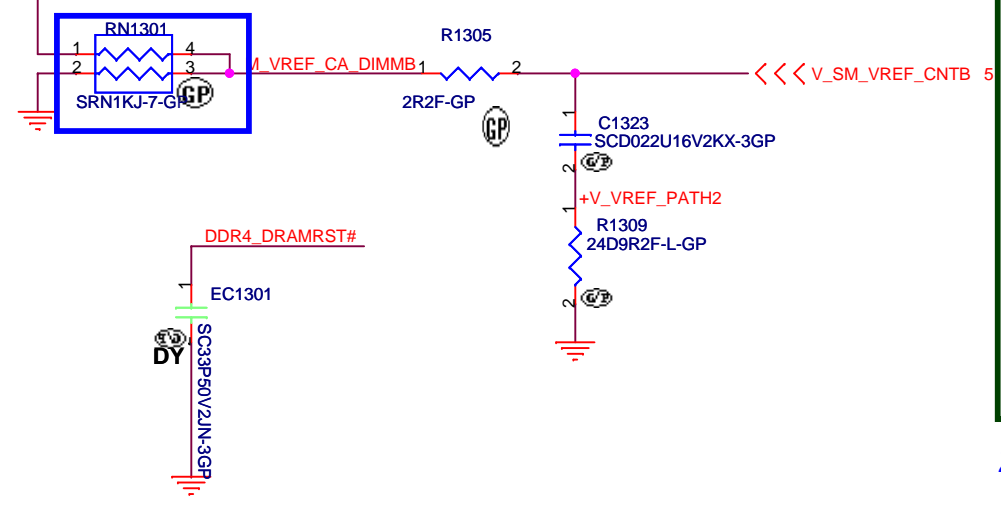
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CPU (Power CAP2)			
Size	Document Number		Rev
A4	OSLO-SKLH		SC
Date:	Wednesday, September 23, 2015	Sheet 11 of	105



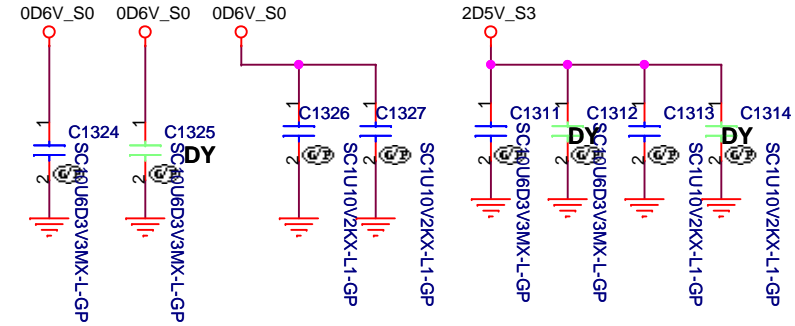
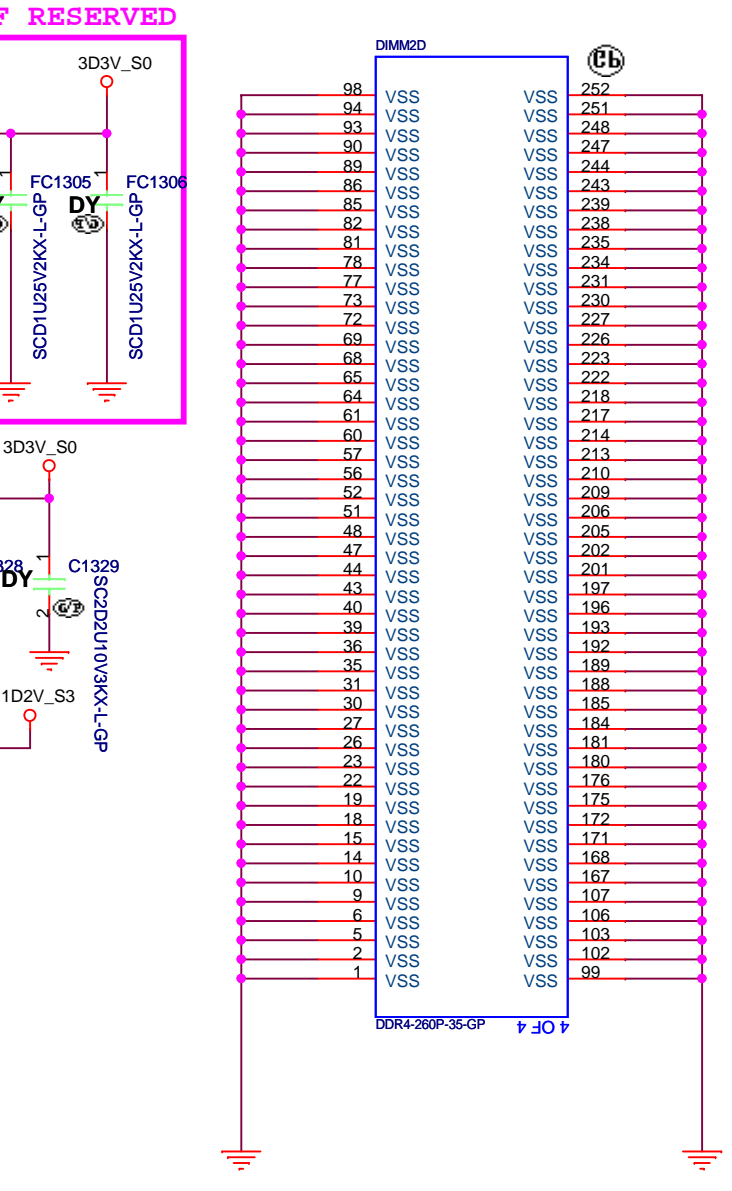
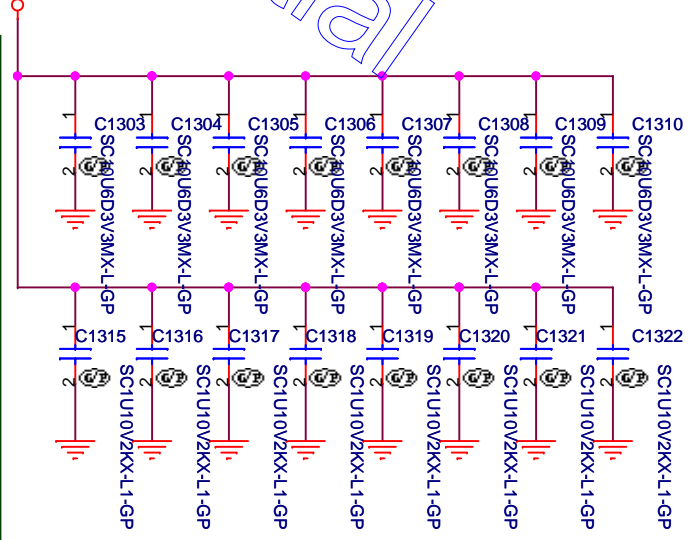
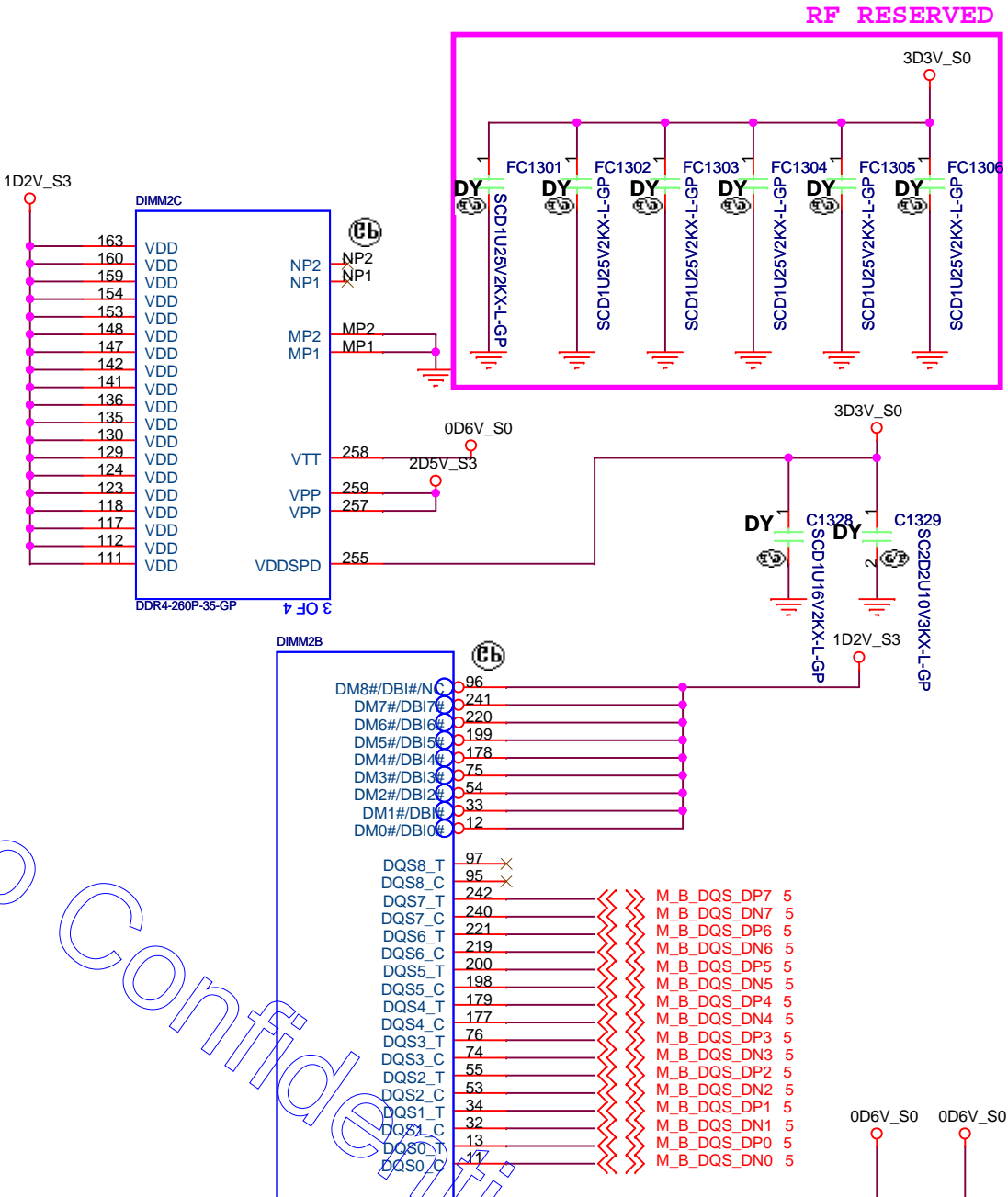
062.10011.0C61

20150813 change PN

20150922 R1301 R1304 change to RN1301

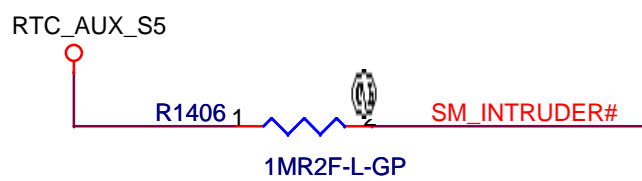
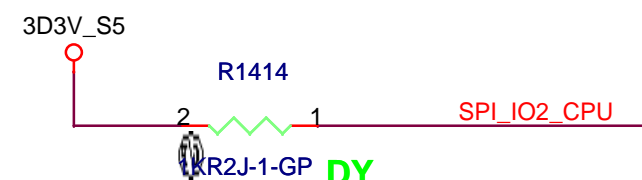
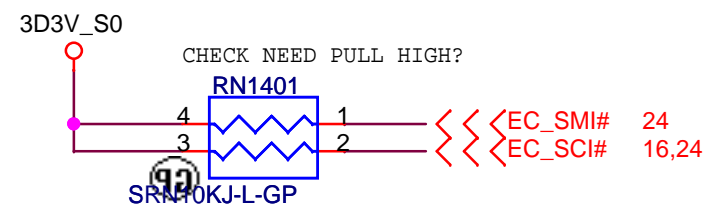
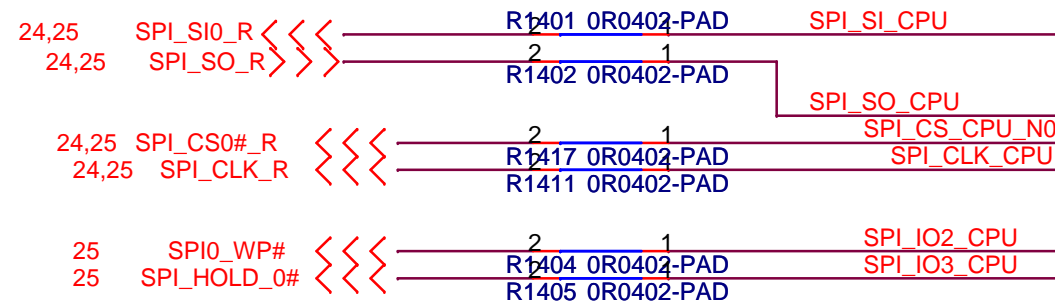


20150821 R1303 R1311 change to PAD

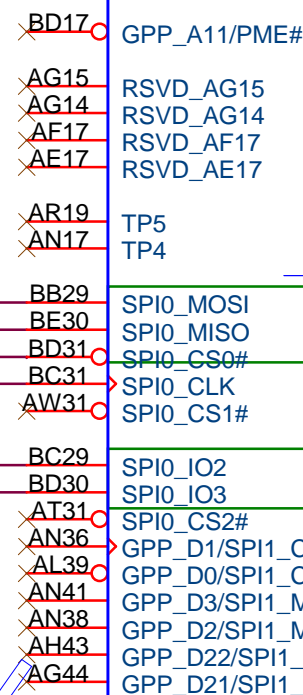


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20150821 R1401 R1402
R1417 R1411 R1404 R1405
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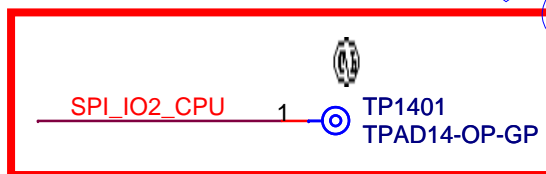


PCH1A



SUNRISE-1-GP

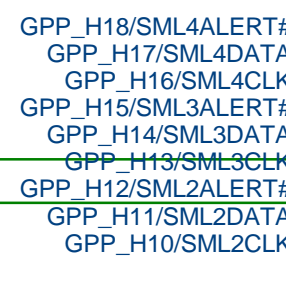
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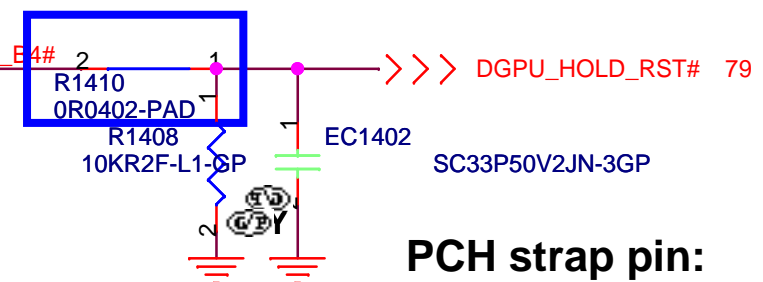
1 OF 12

SPL PCH-H



INTRUDER#

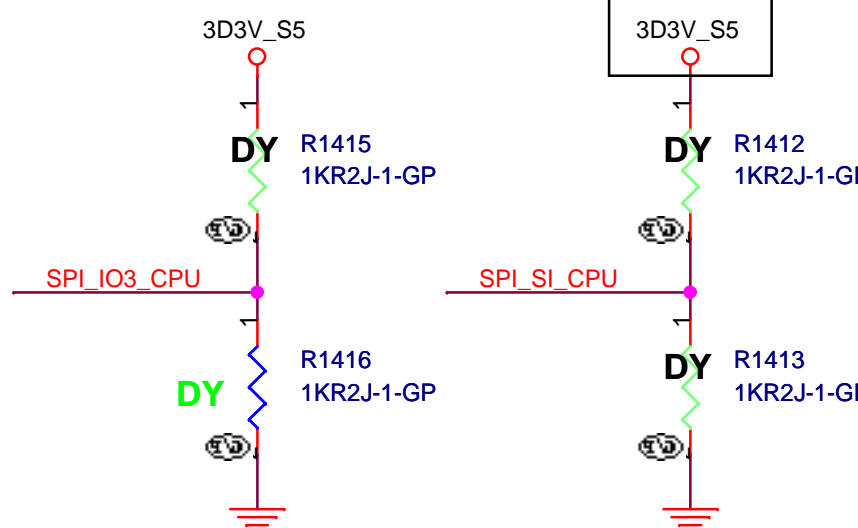
20150821 R1410 change to PAD



BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PCH Prim



05/15 R1416 Change to DY

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Title

PCH_GPP1

Size
A4

Document Number

OSLO-SKLH

Rev

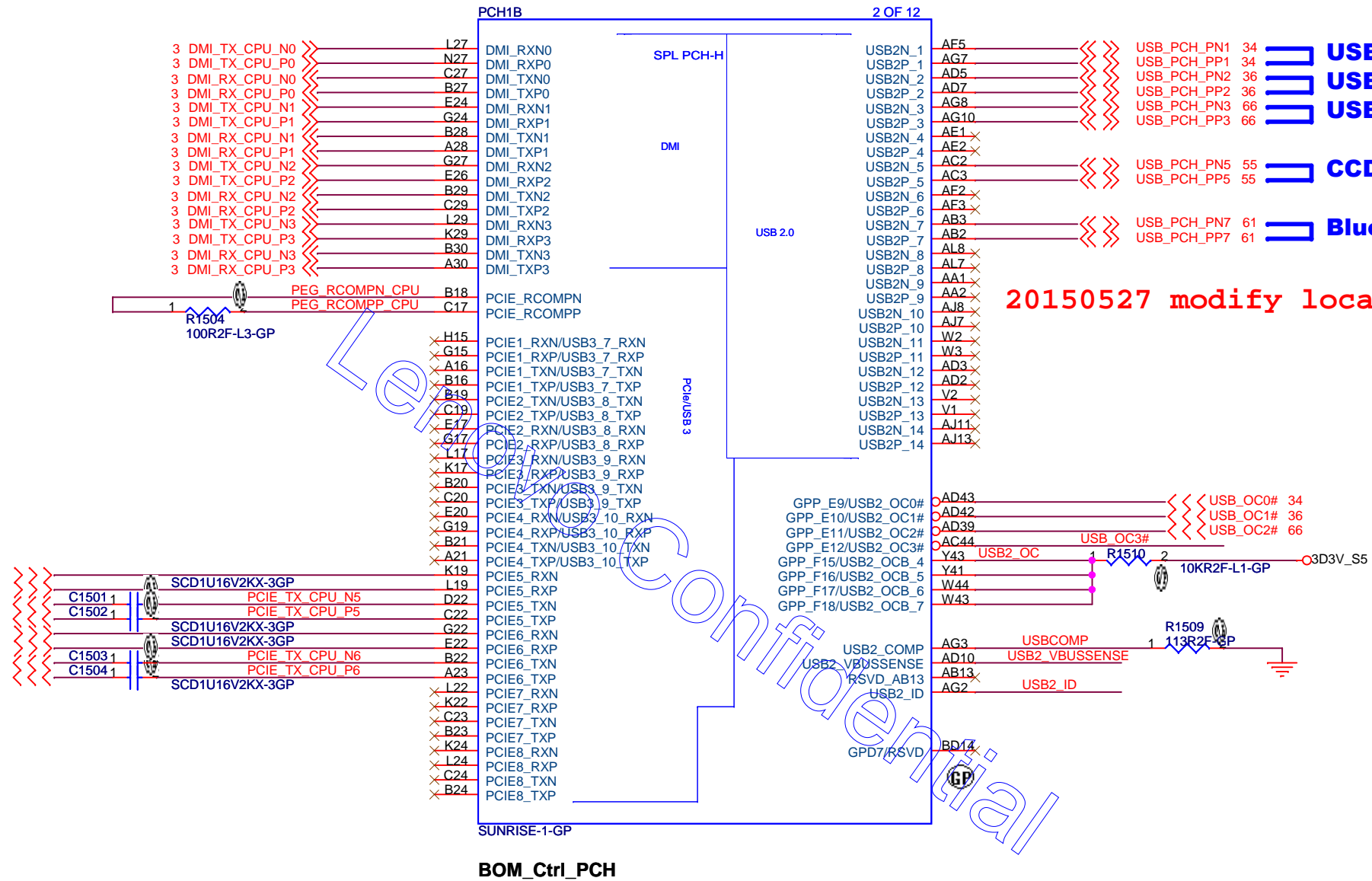
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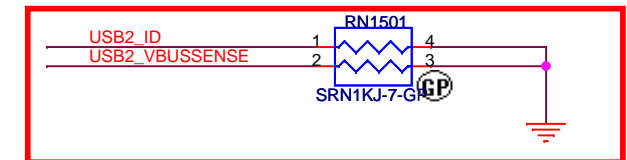
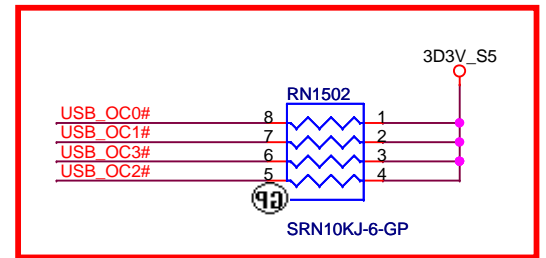
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SSID = PCH

61 PCIE_RX_CPU_N5
61 PCIE_RX_CPU_P5
61 PCIE_TX_CON_N5
61 PCIE_TX_CON_P5
31 PCIE_RX_CPU_N6
31 PCIE_TX_CON_N6
31 PCIE_TX_CON_P6



20150527 modify location name and layout swap



20150527 layout swap

USB Table

Pair	Device
1	USB3.0 Port 1(USB2.0) Charger
2	USB3.0 Port 2(USB2.0)
3	
4	
5	USB2.0
6	
7	Bluetooth
8	Touch Screen
9	CCD
10	Card reader
11	Finger Printer
12	
13	
14	

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SSID = PCH

```
61      CL_CLK
61      CL_DATA
61      CL_RST#
```

EC_SCI# <<<

20150706 remove FW_GPIO

NGFF SSD

NGFF SSD

HDD

NGFF SSD

20150526 NC DEVSLP1_HDD_CON

eDP

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Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	1-15
2. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	16-30
3. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	31-45
4. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	46-60
5. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	61-75
6. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	76-90
7. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	91-105
8. The Impact of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	106-120
9. The Effect of the 1997 Asian Financial Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1	121-135
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PCH PCIE SATA

Size
A4

Document Number

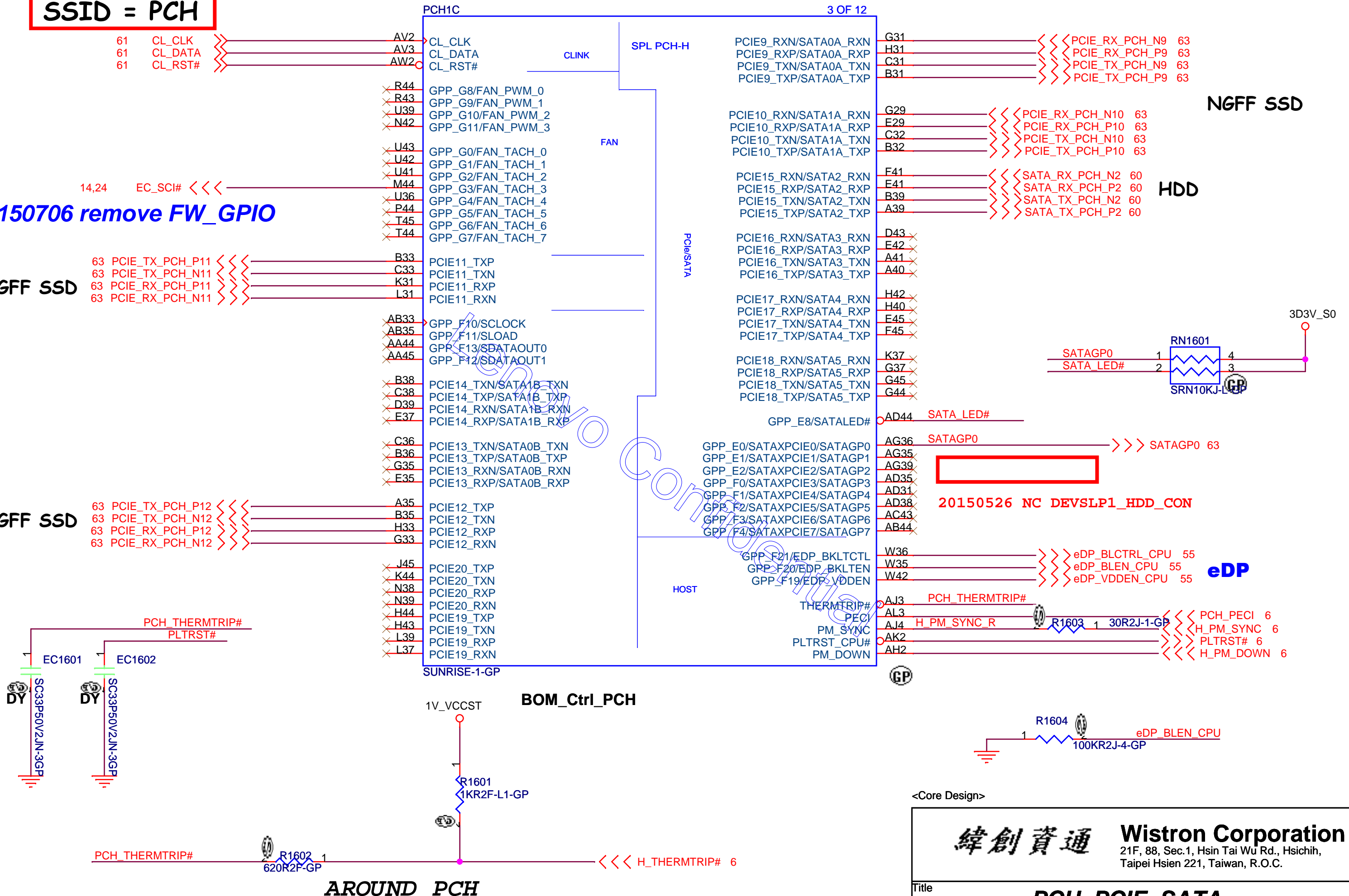
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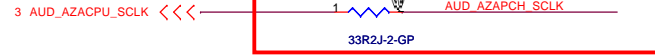
Date: Saturday, July 11, 2015

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05



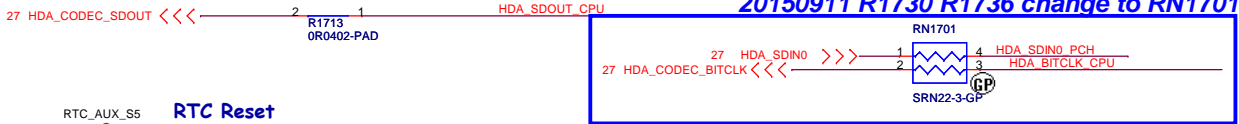
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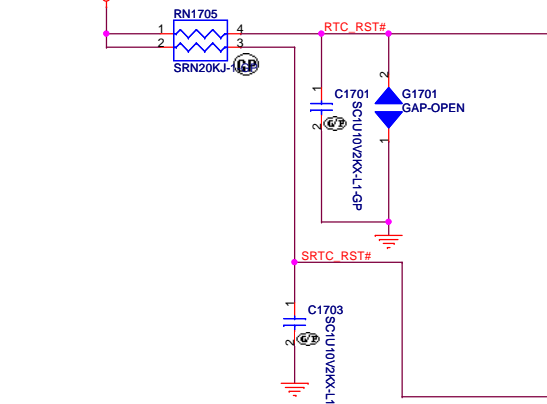
20150529 change to codec 3248

20150821 R1711 R1712 R1714 R1705 R1713 change to PAD

20150911 R1730 R1736 change to RN1701

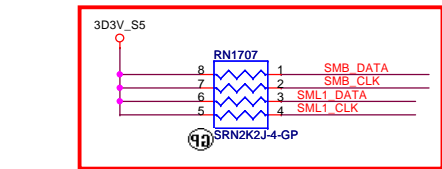


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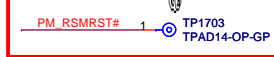
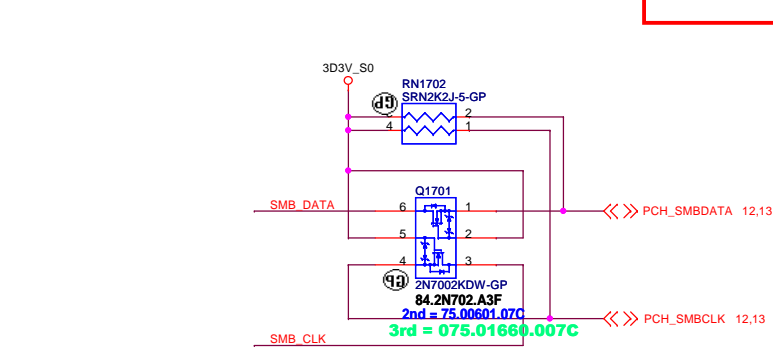


20150911 change C1701 C1703 PN for decap

20150601 ESD reserve



20150527 layout swap



20150526 add TP

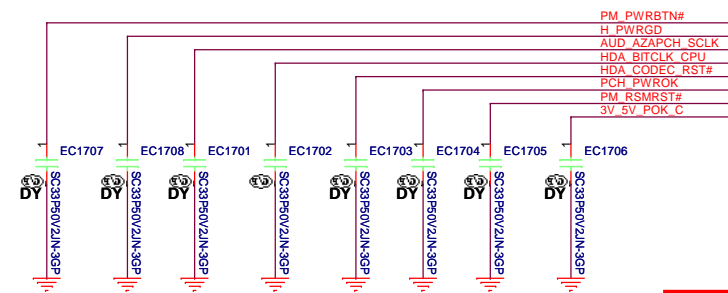


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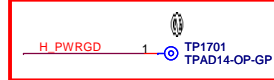


20150604 add TP

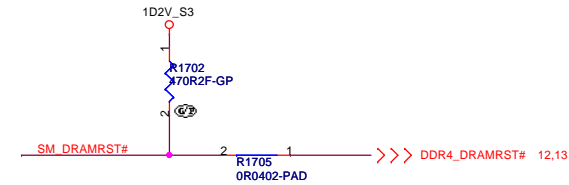
20150828 R1732 change to PAD



20150821 install EC1702 for EMI



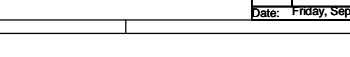
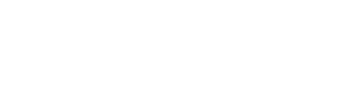
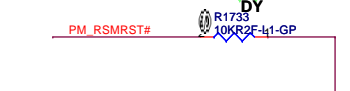
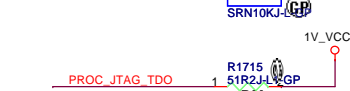
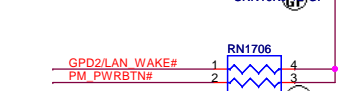
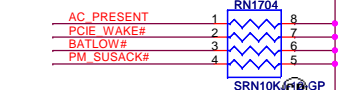
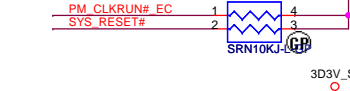
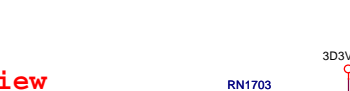
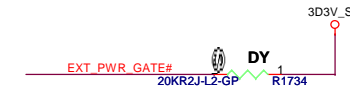
20150525 add TP



20150828 R1706 change to PAD

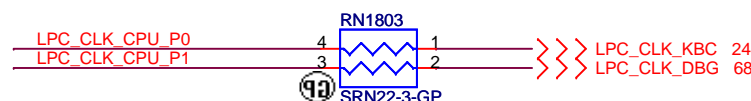
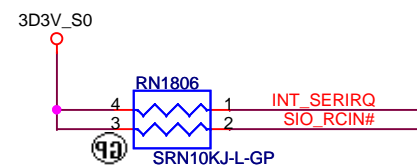
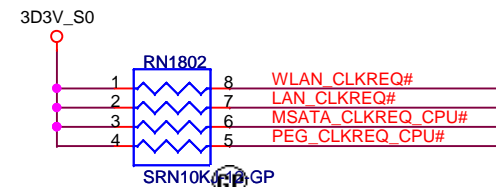
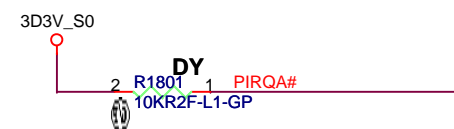
20150527 schematic review

GPU_ALL_PG00D 76



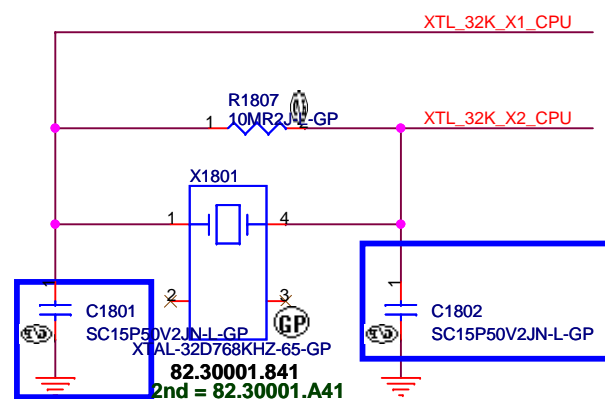
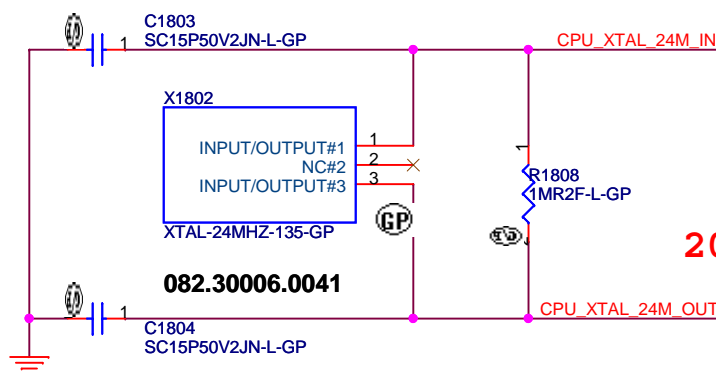
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SSID = PCH



REQ_1 for WLAN
REQ_2 for LAN

20150625 vendor change PN



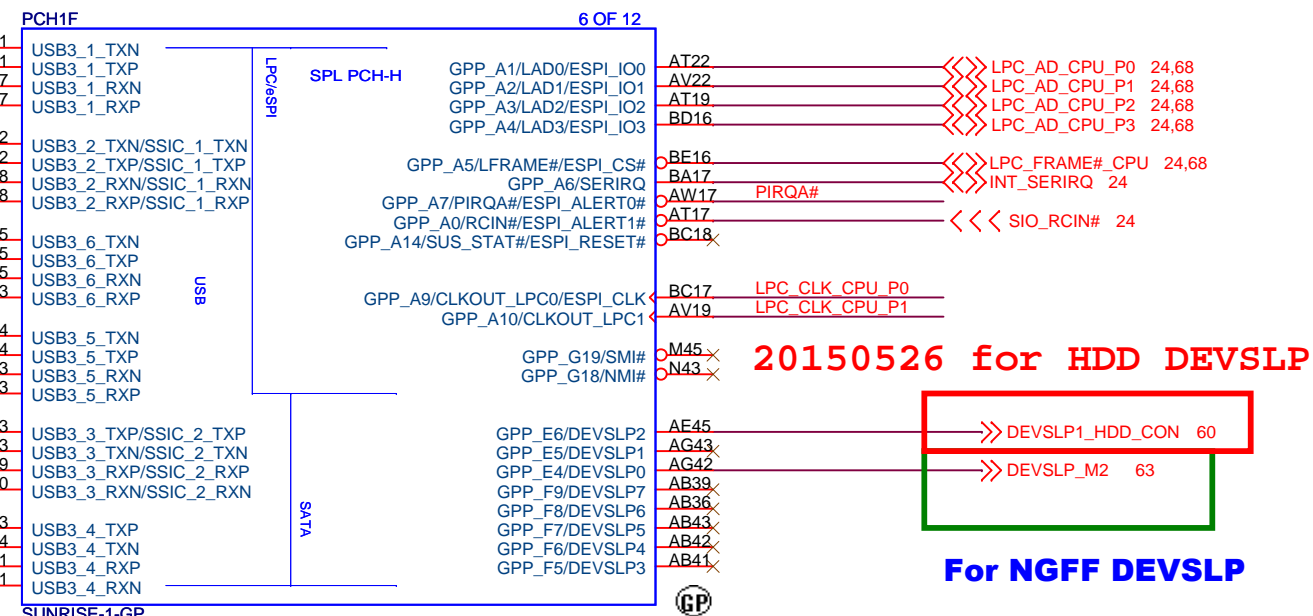
20150825 change to 15P

USB3.0 I/O Port 1

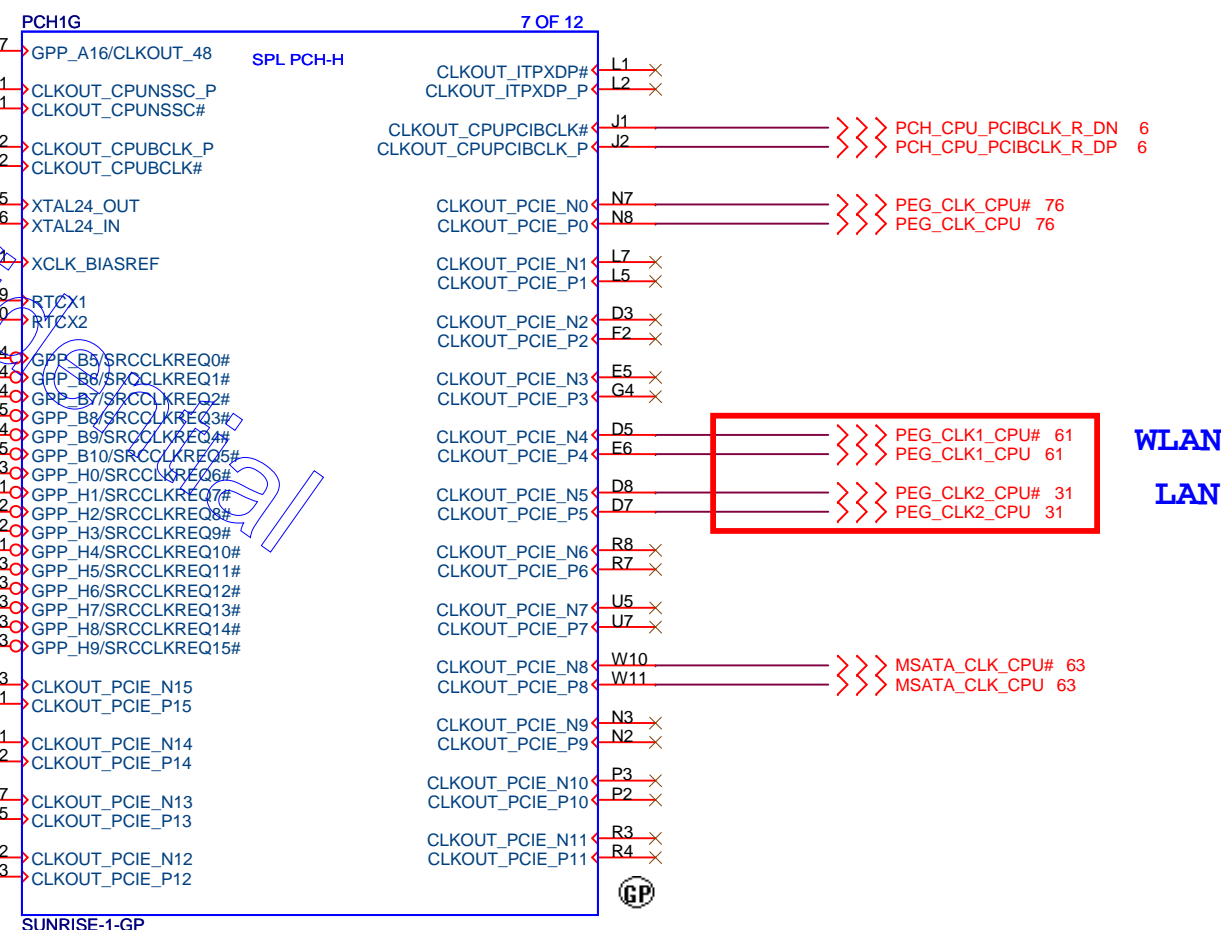
USB3.0 I/O Port 2

Card reader for SD104

20150706 remove 3D camera



BOM_Ctrl_PCH



BOM_Ctrl_PCH

20150604 modify LAN and WLAN port

20150603 remove

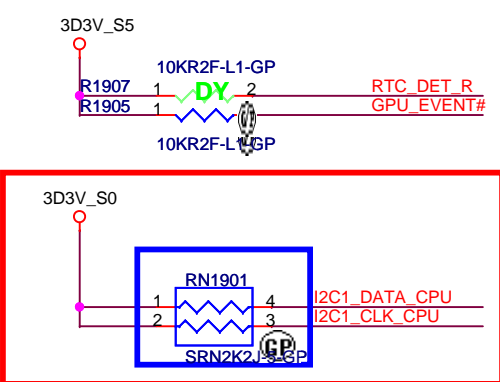
<Core Design>

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Title
PCH USB3 CLOCK
OSLO-SKLH
Size A3 Document Number
Date: Tuesday, August 25, 2015 Sheet 18 of 105
Rev SC

SSID = PCH

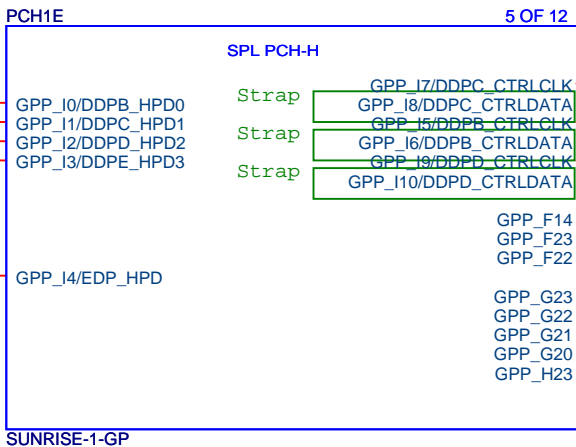
20150703 remove I2C0_CLK_CPU,I2C0_DATA_CPU



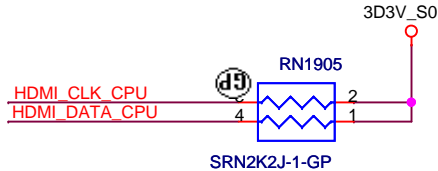
20150527 layout swap

57 HDMI_HPD_CPU >>>

55 EDP_HPD >>>



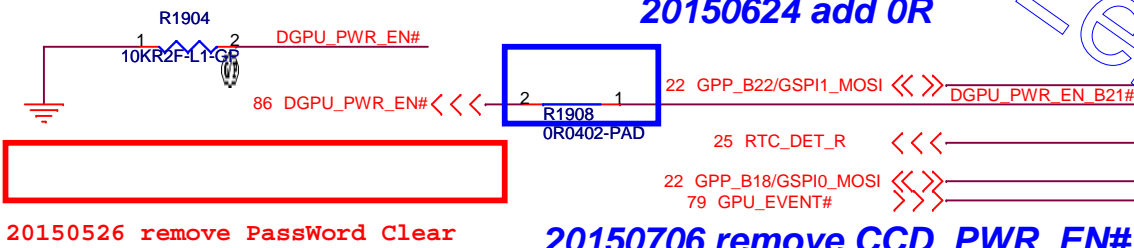
BOM_Ctrl_PCH



20150624 add R1909 R1910 0R

20150911 remove 3D_DETECT

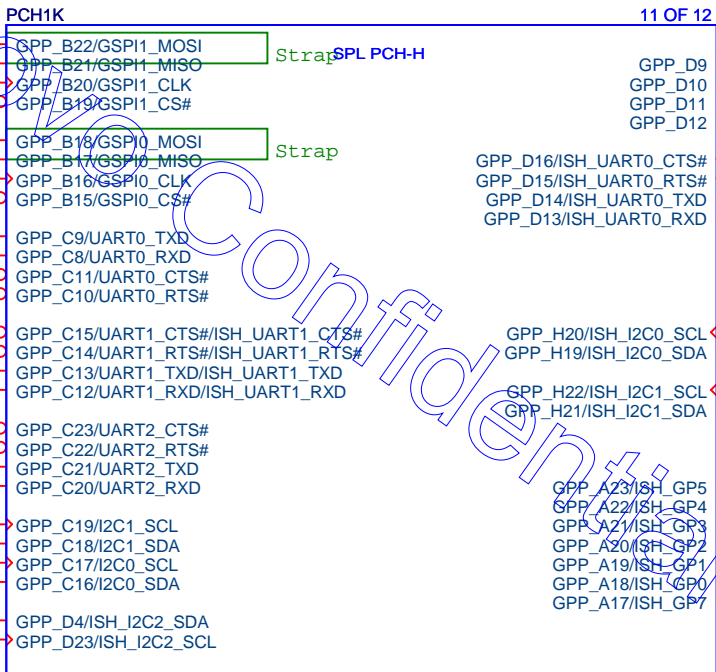
20150624 add 0R



20150526 remove PassWord Clear

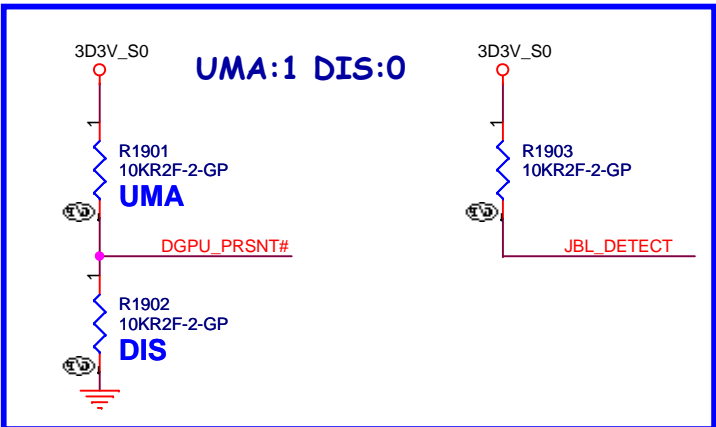
20150706 remove CCD_PWR_EN#

20150821 R1908 change to PAD



BOM_Ctrl_PCH

TOUCH PAD
TOUCH PANEL



20150703 add DGPU_PRSENT# for PCH

JBL:1 NONJBL:0

20150827 DGPU_PRSENT1# change for JBL

20150921 only use R1903 for JBL

<Core Design>

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Title

PCH GPP2 GPP3

Size

Document Number

OSLO-SKLH

Rev

SC

Date: Wednesday, September 23, 2015

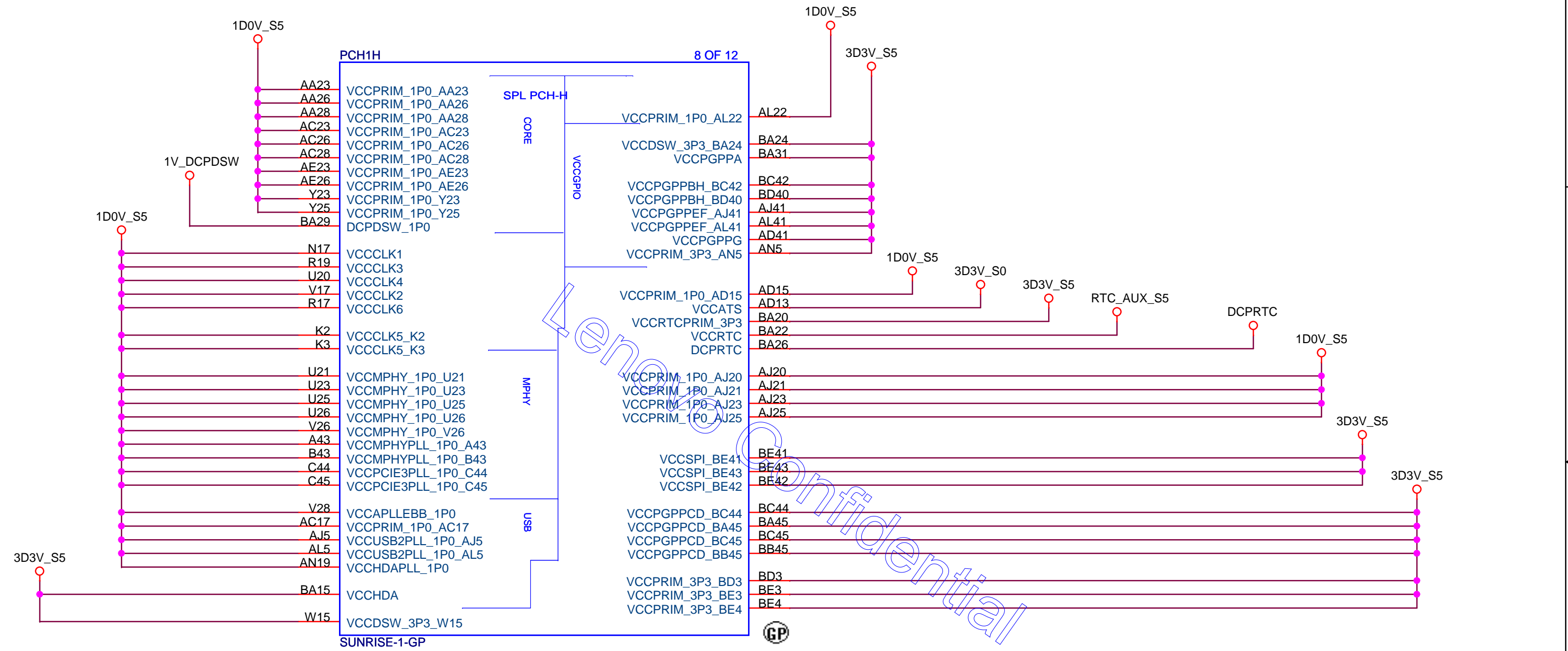
Sheet

19

of

105

SSID = PCH



BOM_Ctrl_PCH

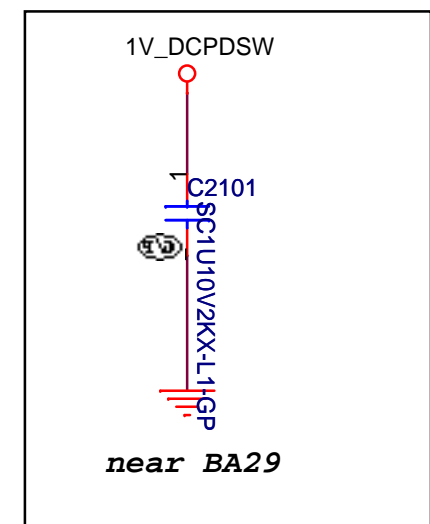
20150911 cancel bead

<Core Design>

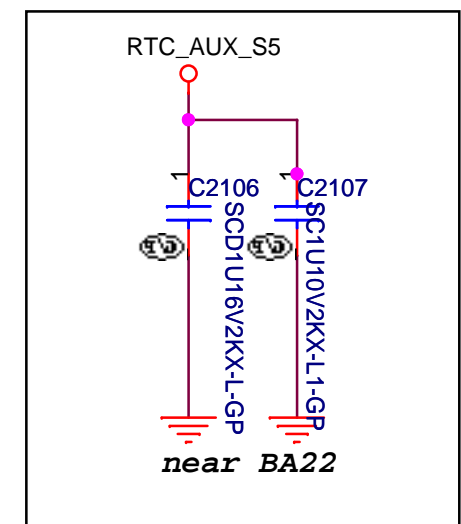
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title PCH_POWER_VCCPRIM_VCCMPHY		
Size A4	Document Number OSLO-SKLH	Rev SC
Date: Friday, September 11, 2015		Sheet 20 of 105

SSID = PCH

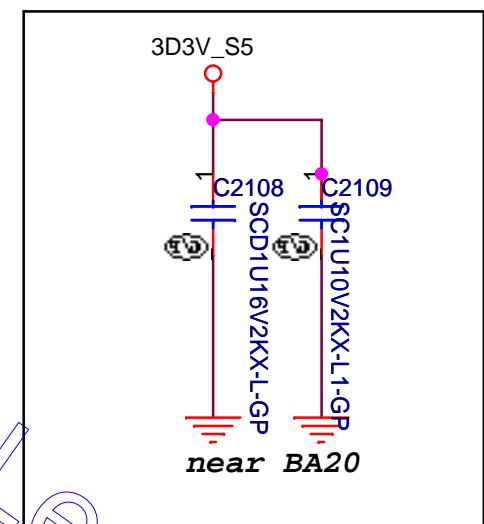
DcpDSW
1x 1uF



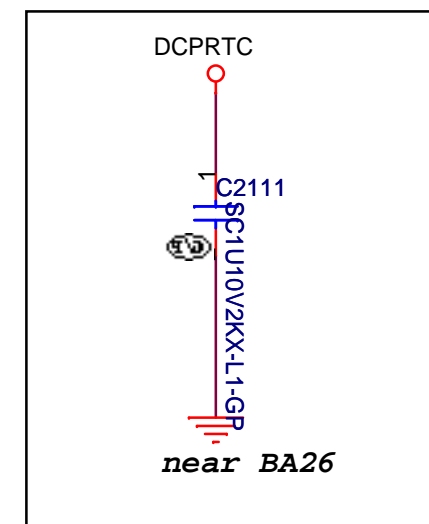
VccRTC
1x1 uF 1x0.1 uF



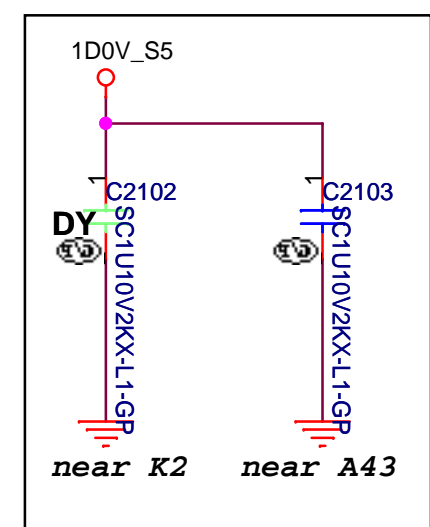
VccRTCPRIM
1x1 uF 1x0.1 uF



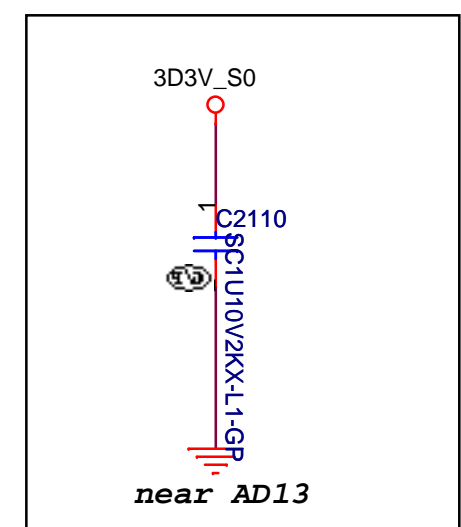
DcpRTC
1x 0.1uF



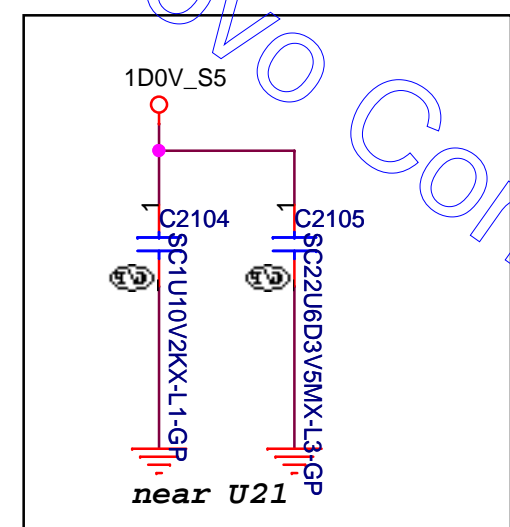
VccMPHYPLL / VccPCIE3PLL
1x1 uF



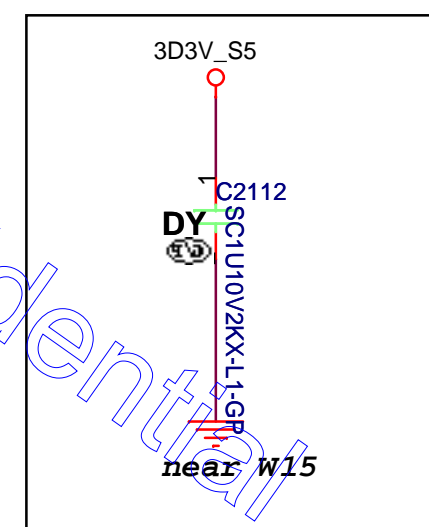
VccATS
1x1 uF



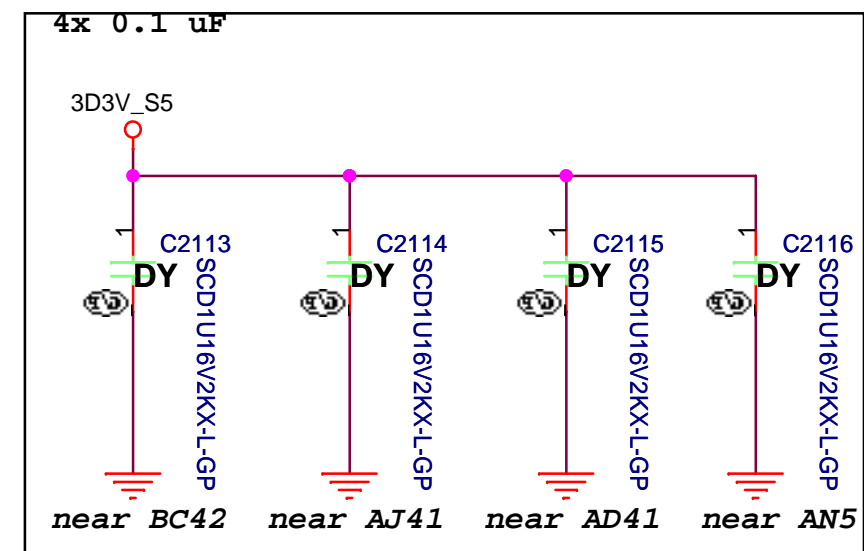
VccMPHY / VccPRIM / VccAPLLEBB
1x1 uF 1x22 uF



VccDSW
1x 1uF



VccPGPPBCH / VccPGPPEF / VccPGPPG
/ VccPRIM
4x 0.1 uF



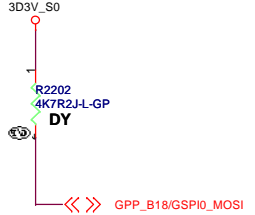
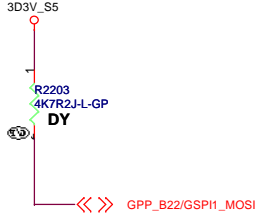
Decoupling and Power Connection Requirements for SKL S/H PCH (DT / AIO)
(Sheet 1 of 2)

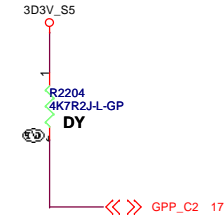
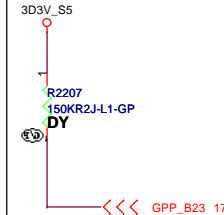
Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R/jumper / E)edge	Place capacitor(s) near ball(s)
V1.0A	VccMPHY	U21, U23, U25,	1 uF	0402	1	E (<3 mm)	U21
	VccPRIM	U26, V26, AC17,	22 uF	0805	1	E (<5 mm)	
	VccAPLLEBB	V28					
	VccMPHYPLL	A43, B43, C44,	1 uF	0402	1	E (<5 mm)	A43
	VccPCIE3PLL	C45					
	VccCLK5	K2, K3	1 uF	0402	1	E (<5 mm)	K2 (Note 1)
	VccCLK (1,2,3,4,6)	N17, R19, U20, V17, R17	-	-	-	-	-
	VccUSB2PLL	A15, AL5, AN19	-	-	-	-	-
V1.0A	VccHDAPLL	AJ5, AJ5, AN19	-	-	-	-	-
	VccPRIM	AL22	-	-	-	-	-
	VccPRIM	AD15	-	-	-	-	-
	VccPRIM	AJ20, AJ21, AJ23, AJ25	-	-	-	-	-
	VccPRIM	AA23, AA26, AA28, AC23, AC26, AC28, AE23, AE26, Y23, Y25	-	-	-	-	-
	VccPRIM		-	-	-	-	-
V1.0DS W	DcpDSW	BA29	1 uF	0402	1	E (<5 mm)	BA29
V1.8A/ V3.3A	VccPGPPBCH	BC42, BD40	0.1 uF	0402	1	E (<3 mm)	BC42 (Note 1)
	VccPGPPEF	AJ41, AL41	0.1 uF	0402	1	E (<3 mm)	AJ41 (Note 1)
	VccPGPPG	AD41	0.1 uF	0402	1	E (<3 mm)	AD41 (Note 1)
	VccPRIM	AN5	0.1 uF	0402	1	E (<3 mm)	AN5 (Note 1)
	VccGPRA	BA31	-	-	-	-	-
	VccSPI	BE41, BE42, BE43	-	-	-	-	-
V1.8A/ V1.85/ V3.3S	VccGPPD	BC44, BA45, BC45, BB45	-	-	-	-	-
	VccATS	AD13	1 uF	0402	1	E (<5 mm)	AD13
V1.5A/ V1.8A/ V3.3A	VccHDA	BA15	-	-	-	-	-
V3.3A	VccRTCPRIM	BA20	1 uF	0402	1	E (<5 mm)	BA20
	VccPRIM	BD3, BE3, BE4	-	-	-	-	
V3.3RTC	VccRTC	BA22	1 uF	0402	1	E (<5 mm)	BA22
	VccRTC	BA22	0.1 uF	0402	1	E (<3 mm)	
V3.3DS W	VccDSW	W15	1 uF	0401	1	E (<3 mm)	W15 (Note 1)
	VccDSW	BA24	-	-	-	-	-
PCH Internal VRM	DcpRTC	BA26	0.1 uF	0402	1	E (<5 mm)	BA26

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Title PCH_POWER_CAP1		
Size A4	Document Number OSLO-SKLH	Rev SC
Date: Saturday, July 11, 2015		Sheet 21 of 105

Description	Display Port B Detected	Display Port C Detected	Display Port D Detected	No reboot	Boot BIOS strap bit BBS	Flash descriptor security override	ESPI FLASH SHARING MODE
GPIO	GPP_I6	GPP_I8	GPP_I10	GPP_B18	GPP_B22	HDA_SDO	GPP_H12
Schematic	Pull up at p.71 RN7101						
High	Detected	Detected	Detected	Enable	LPC	Disable	1:SLAVE ATTACEHD FLASH SHARING ESPI FLASH SHARING MODE
Low	Not Detected	Not Detected	Not Detected	Disable	SPI	Enable	0: MASTER ATTACHED FLASH SHARING
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down

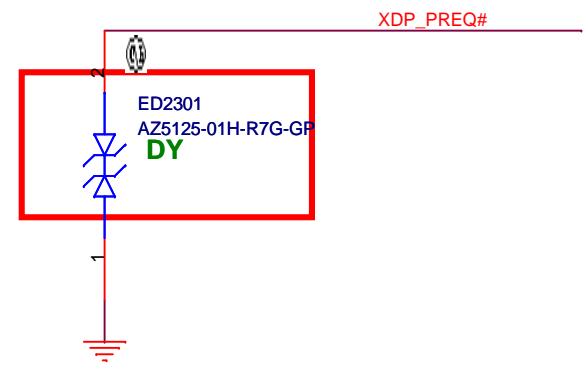
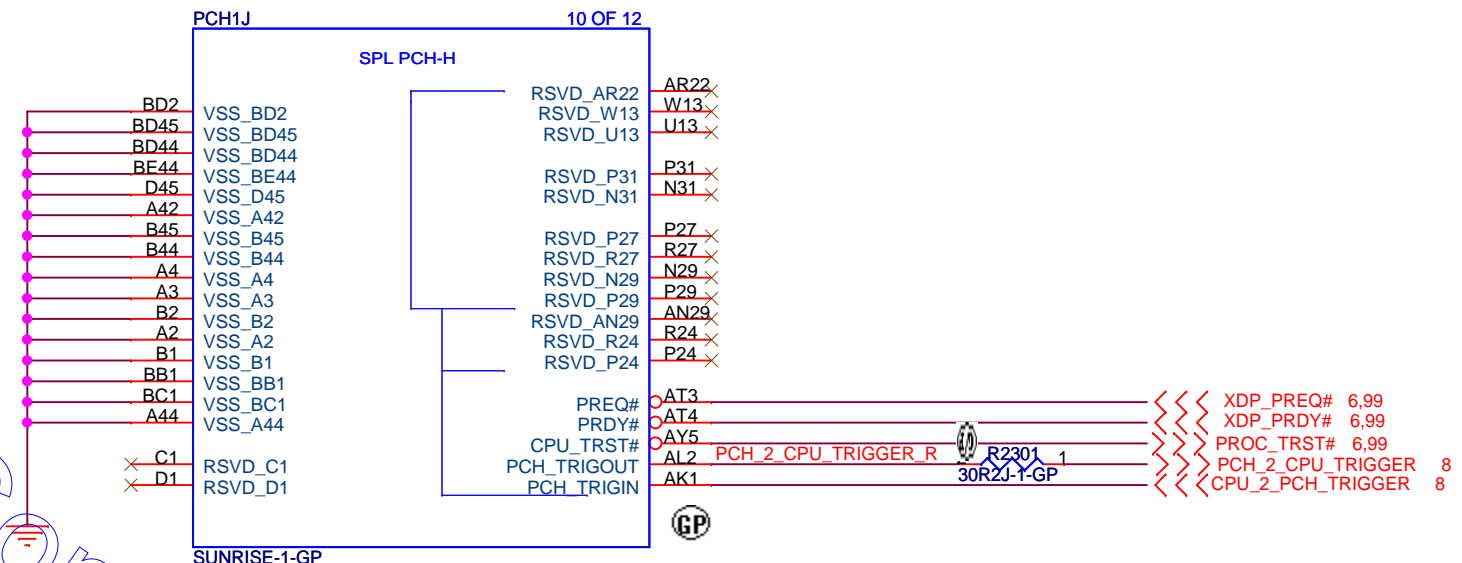
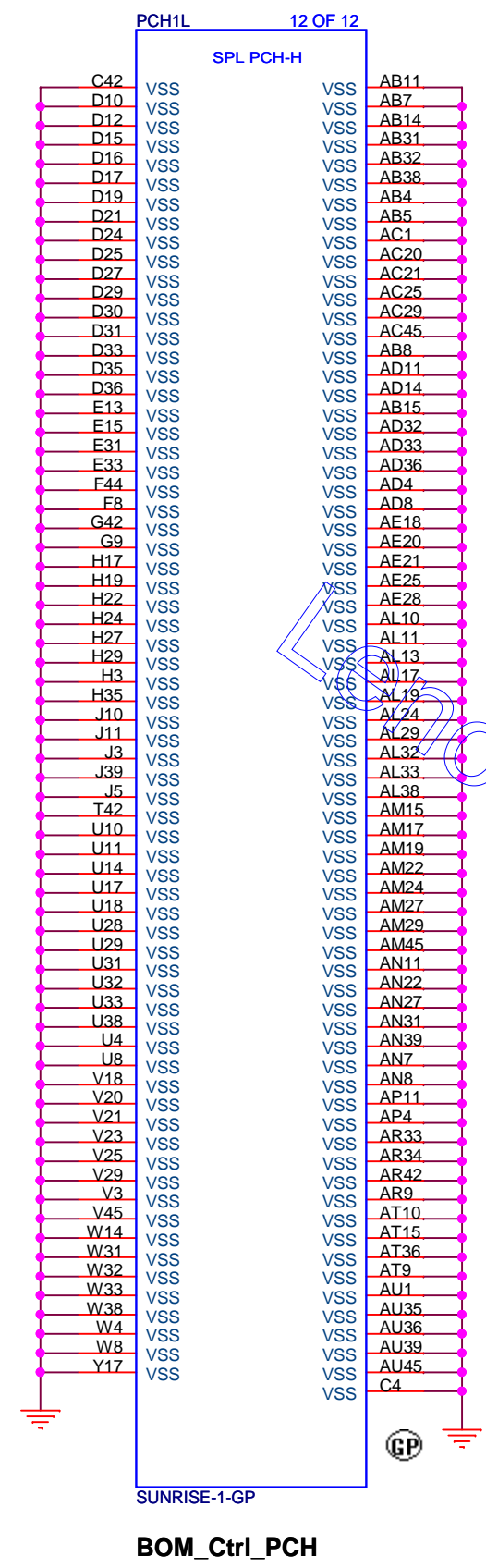
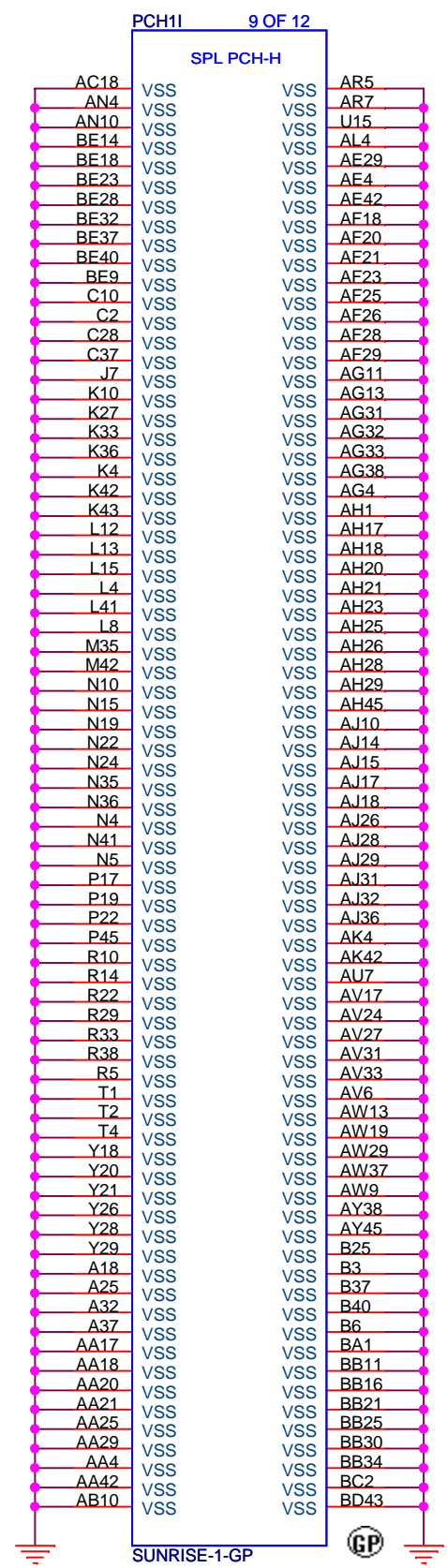
Description	Top Swap Override	eSPI or LPC	TLS Confidentiality	Reserved	Reserved	Reserved	Reserved	Reserved
GPIO	GPP_B14	GPP_C5	GPP_C2	SPI0_IO3	SPI0_IO2	SPI0_MOSI	SPI0_MISO	GPP_B23 / PCHHOT#
Schematic								
High	Enable	eSPI	Enable					
Low	Disable	LPC	Disable					
	internal pull-down	internal pull-down	internal pull-down	internal pull-up	internal pull-up	internal pull-up	internal pull-up	internal pull-down

[H,S,U,Y] Pull-up Resistors on SPI_IO2 and SPI_IO3 Requirement Update

The current Skylake Platform Design Guide (PDG) states that a 1 K pull-up resistor is required on the PCH SPI_IO2 and SPI_IO3 signals

This 1K pull up resistor is no longer needed on Skylake platforms and can be removed from the motherboard. The new guidelines will be updated in a future release of the Skylake PDG

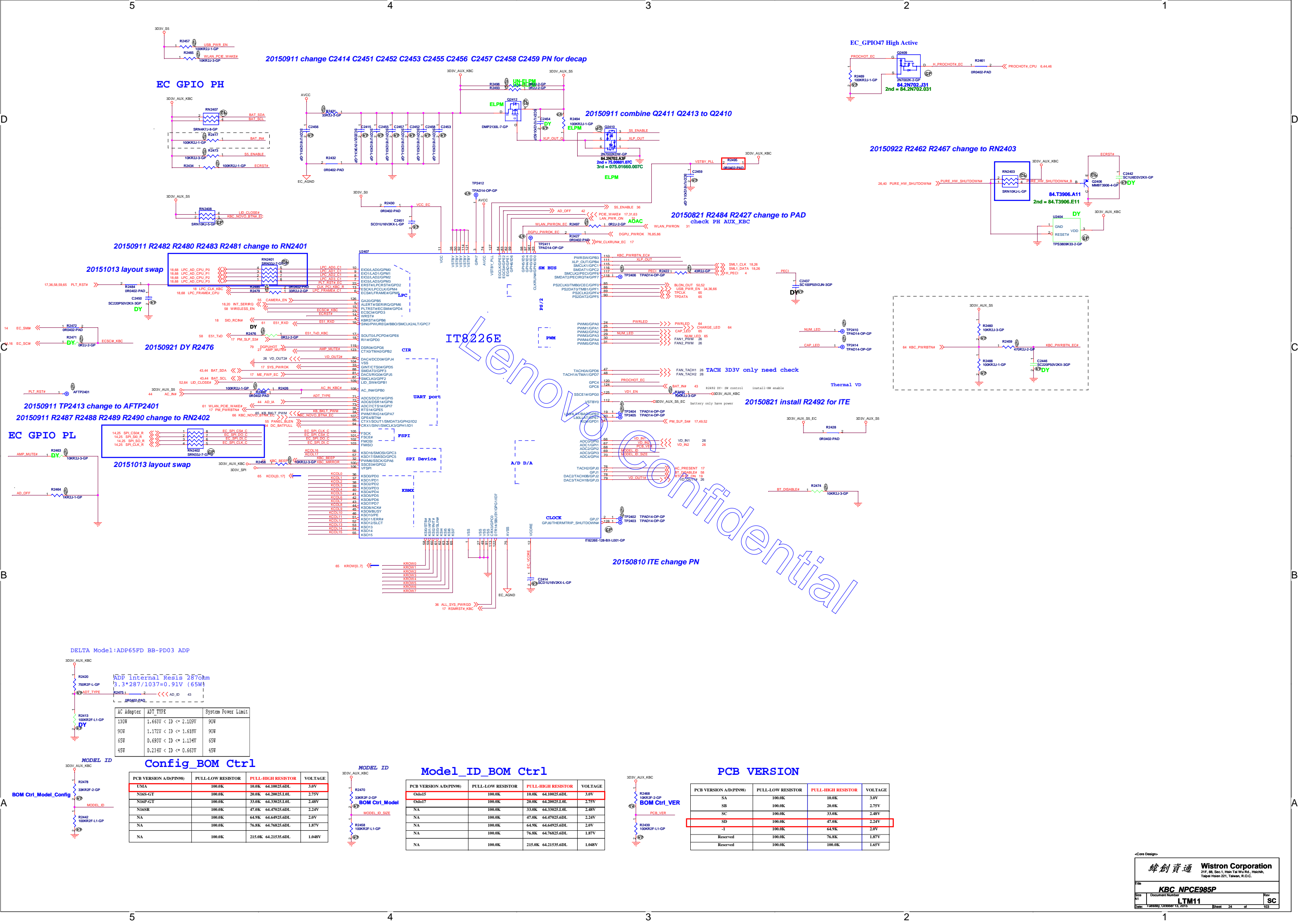
SSID = PCH



20150601 ESD reserve

<Core Design>

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Title PCH_RSVD_VSS		
Size B	Document Number OSLO-SKLH	Rev SC
Date: Saturday, July 11, 2015	Sheet 23	of 105



SSID = Flash.ROM

U2502			
Main	Winbond		72.25128.0E1
SC			
SD			

SPI ROM Equal length need to less than 500mil

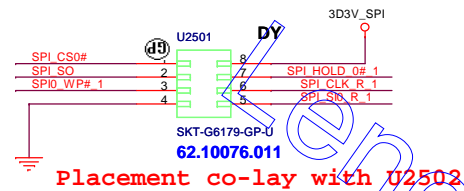
20150617 ITE review

20150911 TP2503 change to AFTP2501

20150911 R2503 R2550 change to RN2501

20150821 R2502 chang to PAD

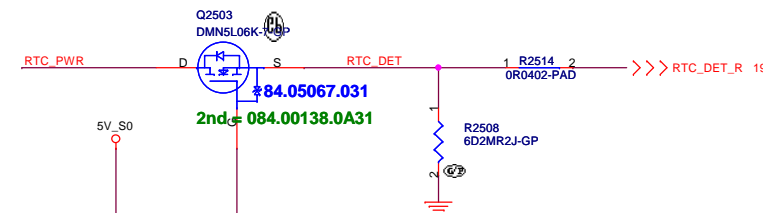
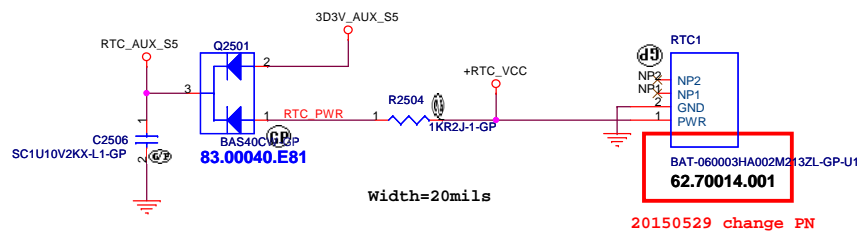
SPI ROM Equal length need to less than 500mil



SSID = RBATT

SSID = RBATT

High Detect
Need to Check whether to PD in PCH Side



20150528 modify to TP

20150911 TP2501 change to AFTP2502

<Core Design>

ALERT#	/T CRIT#
Pull-up	R _{esistor}

5V_FAN_S0

D2601
RB551V30-GP

C2604
SC107J250-BKX-L2

C2605
SCD1U16V2KK-L-GP

83.R5003.H8B

2nd = 83.R5003.N8F

	R7				
	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
R5					
2Kohm	77°C	87°C	97°C	107°C	117°C
7.5Kohm	79°C	89°C	99°C	109°C	119°C
10.5Kohm	81°C	91°C	101°C	111°C	121°C
14Kohm	83°C	93°C	103°C	113°C	123°C
18.7Kohm	85°C	95°C	105°C	115°C	125°C

T_CRIT temperature strapping point

Pin 10 connection diagram for the ACES 68865-GP module. The diagram shows a 10-pin connector labeled FAN1. Pin 1 is connected to FAN2_PWM. Pin 2 is connected to FAN_TACH2_C. Pin 3 is connected to FAN2_PWM. Pin 4 is connected to FAN2_PWM. Pin 5 is connected to FAN1_PWM. Pin 6 is connected to FAN1_TACH1_C. Pin 7 is connected to FAN1_PWM. Pin 8 is connected to FAN1_PWM. Pin 9 is connected to FAN1_PWM. Pin 10 is connected to 5V_FAN_S0. The module is labeled ACES 68865-GP and has a part number 020.F0256.0008.

[illegible]

06/11 Delete R2611 & R2621 Connect to 3D3V_AUX_S5

Thermal config

Note: (1) VD_IN1 for CPU
(2) VD_IN2 for System

Close to CPU chips

Close to KBC chips

TBD PU 3D3V_AUX_KBC

TBD PU 3D3V_AUX_KBC

3D3V_AUX_KBC

R2615 16KR2F-GP

R2610 NTC-100K-11-GP-UJ 69.60013.201

C2615 SCD1U16V2KX-L-GP

C2616 SC100P50V2JN-3GP

VD_IN1 C

R2612 0R0402-PAD

VD_IN1 24

3D3V_AUX_KBC

R2616 16KR2F-GP

R2619 NTC-100K-11-GP-UJ 69.60013.201

C2617 SCD1U16V2KX-L-GP

C2618 SC100P50V2JN-3GP

VD_IN2 C

R2620 0R0402-PAD

VD_IN2 24

20150911 R2614 R2621 change to RN2602

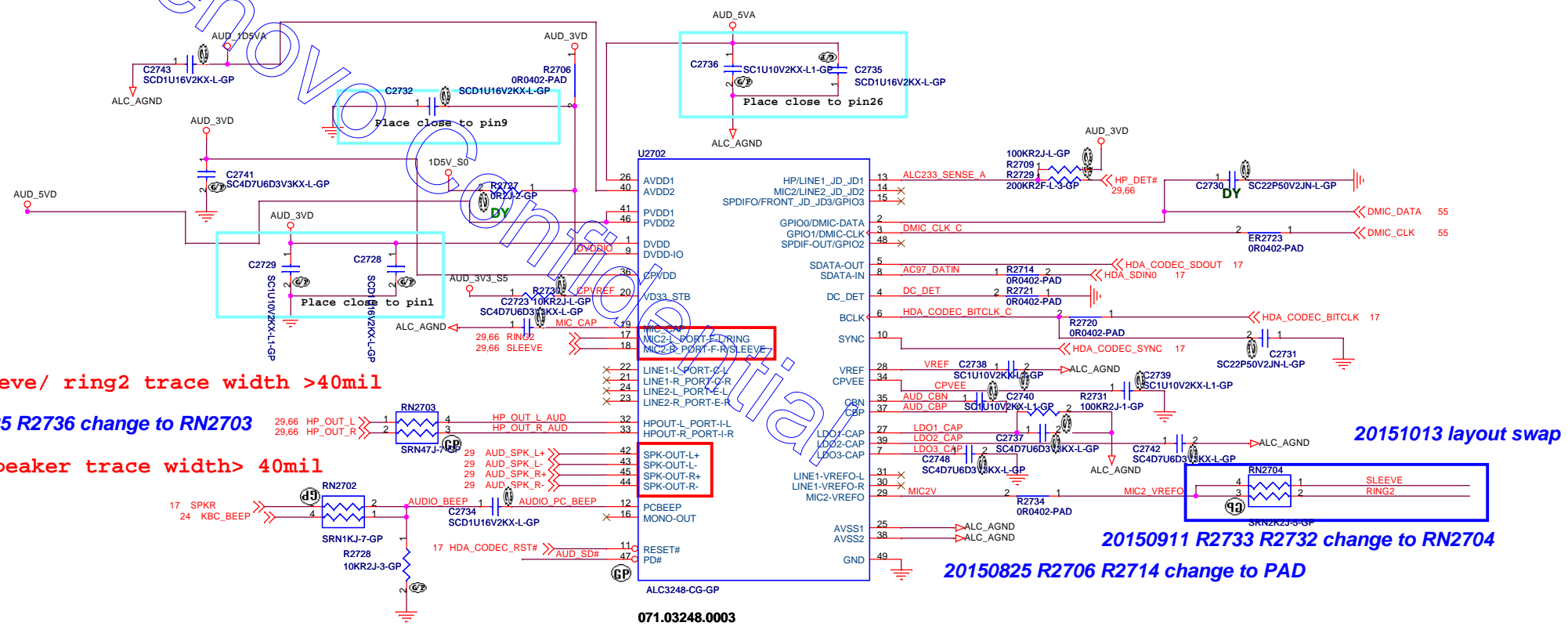
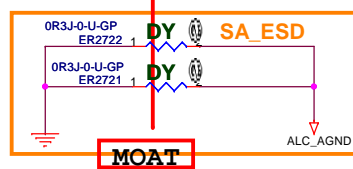
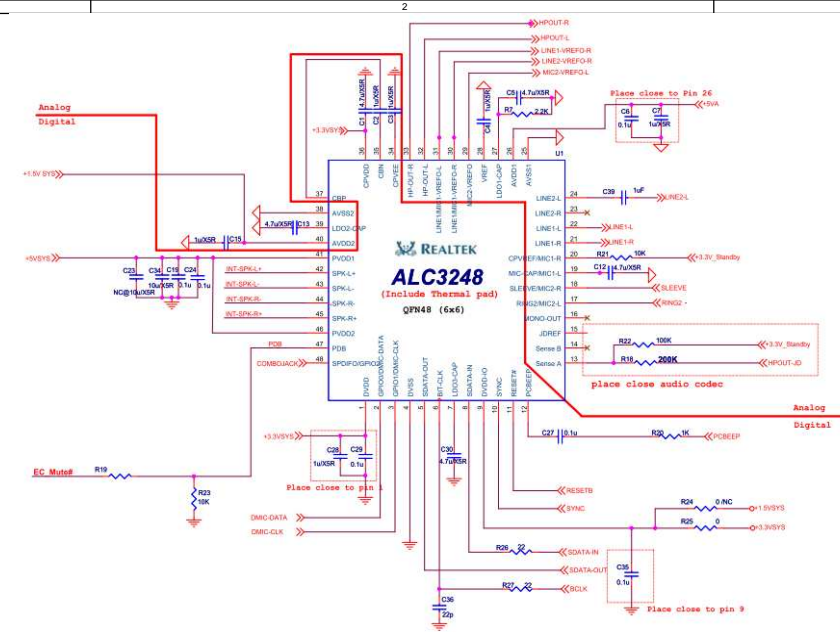
20150701 modify FAN pin define

20150821 R2607 change to 10K, R2624 R2625 DY for ITE review

20150617 install R2624,R2625,D2603,DY R2617

T8=85 degree

Function LOCATION	Thermal VD	NCT7718W
U2601	DY	ASM
Q2601	DY	ASM
Q2602	DY	ASM
RN2601	DY	ASM
R2601	DY	ASM
R2605	DY	ASM
C2601	DY	ASM
C2602	DY	ASM
C2603	DY	ASM
R2610	ASM	DY
R2619	ASM	DY
R2615	ASM	DY
R2616	ASM	DY
R2612	ASM	DY
R2620	ASM	DY
R2624	ASM	DY
R2625	ASM	DY
C2615	ASM	DY
C2617	ASM	DY
C2616	ASM	DY
C2618	ASM	DY
D2603	ASM	DY
RI717	ASM	DY



Title			
Audio Codec ALC3248			
Size A2	Document Number		Rev
	OSLO-SKLH		SC
Date:	Tuesday, October 13, 2015		Sheet 27 of 105

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

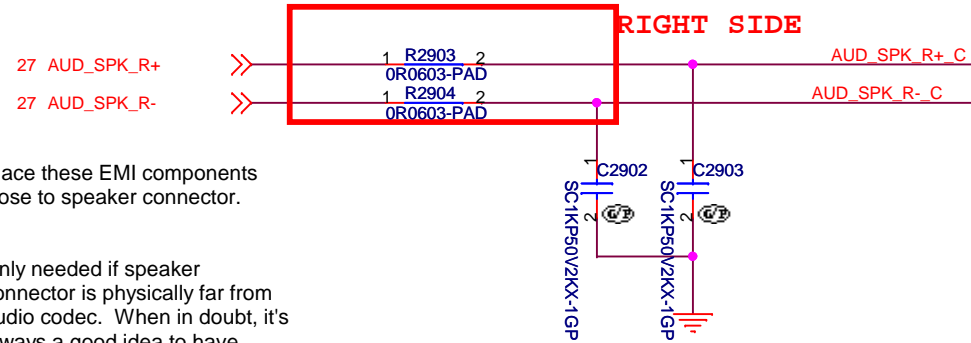
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<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
<div>(Reserved)</div>			
Size A4	Document Number		Rev
	OSLO-SKLH		SC
Date:	Saturday, July 11, 2015	Sheet 28 of	105

INTERNAL STEREO SPEAKERS

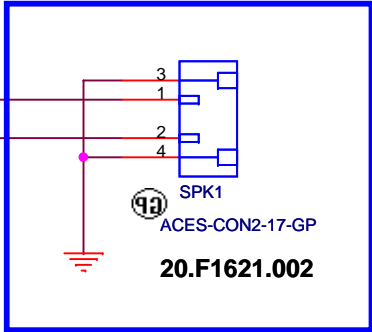
20150603 change from shortpad to 0R



Place these EMI components close to speaker connector.

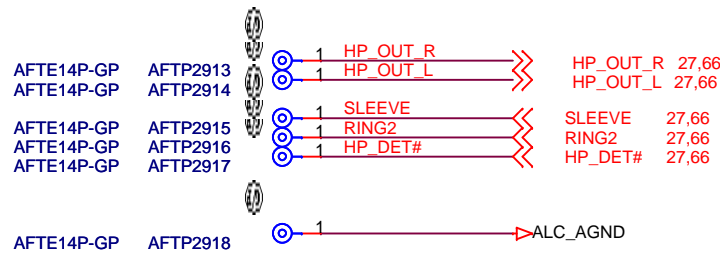
Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.

20150630 SPK change to 2pin



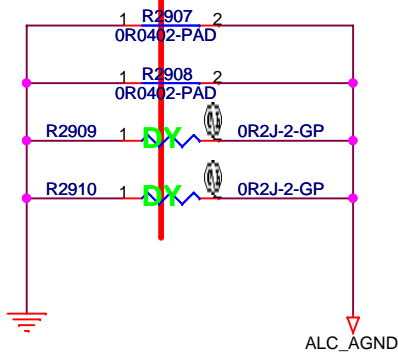
20150821 R2903 R2904 change to PAD

08/12 SPK1 20.F2348.007 Change to 20.F1621.004
06/12 SPK1 原本為4Pin, 換7 pin 接 Hall Sensor 訊號

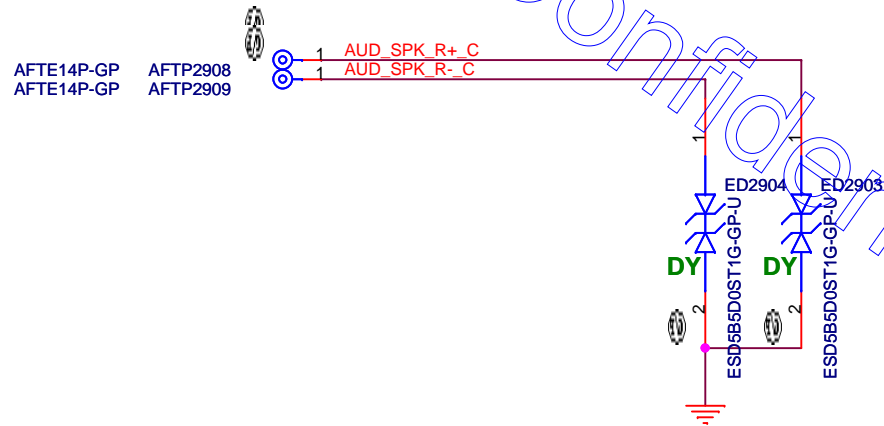
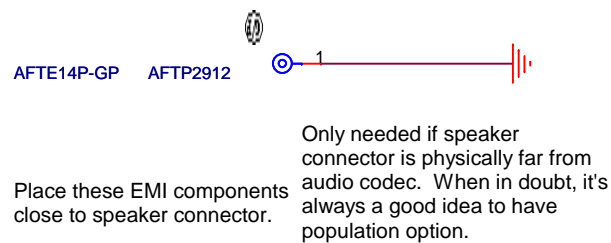


MOAT

20150602 MOAT



20150706 remove ED2901,ED2902



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio IO

Size
A3

Document Number

OSLO-SKLH

Rev
SC

Date: Friday, August 21, 2015

Sheet 29 of 105

D

C

B

A

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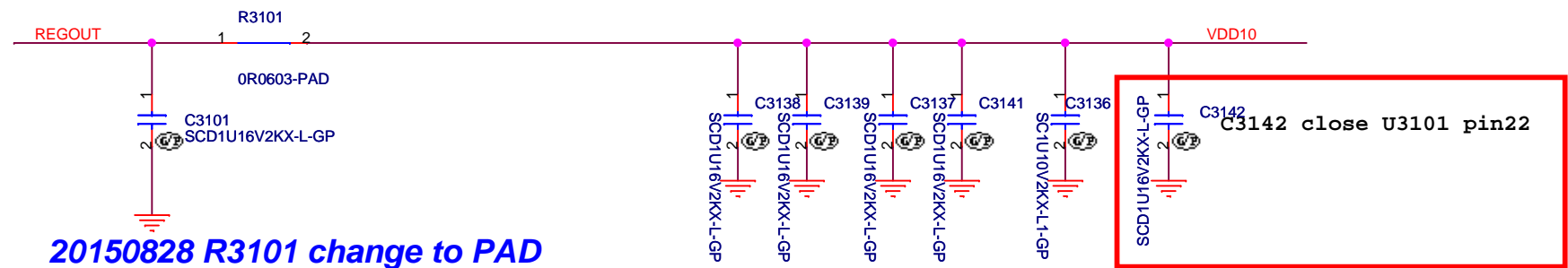
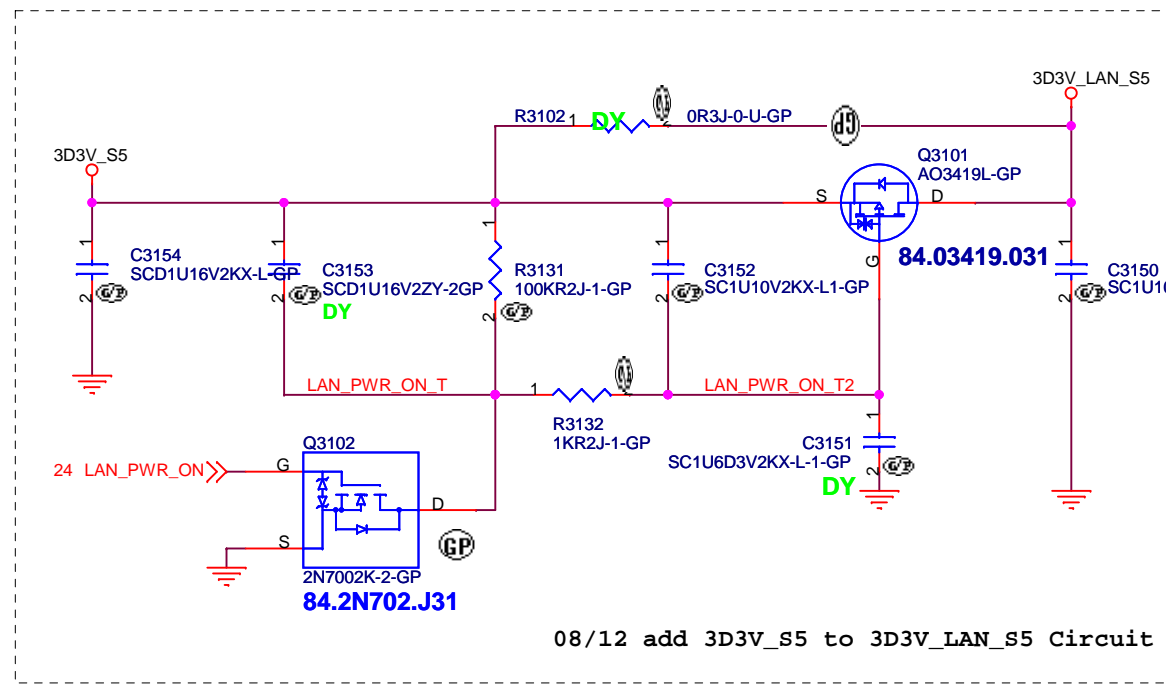
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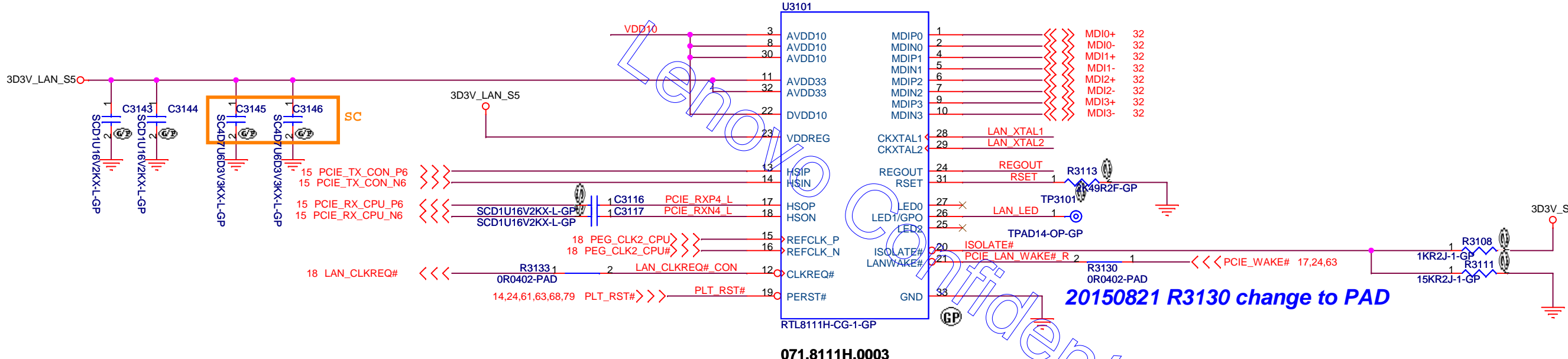
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Size A	Document Number OSLO-SKLH	Rev SC
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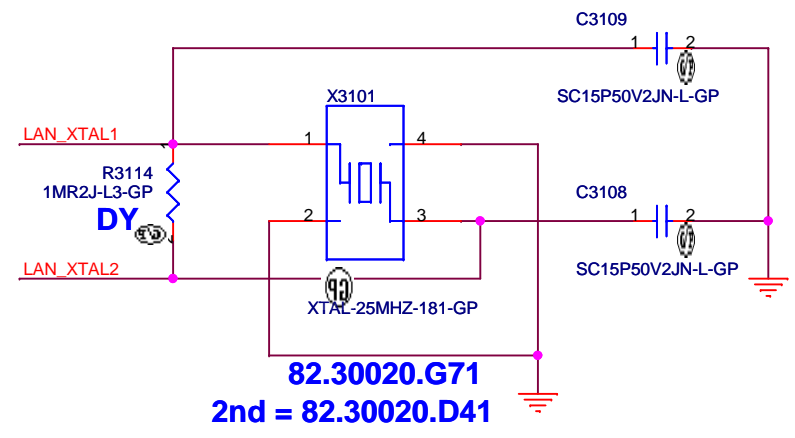


	1.0 V source	Lx	Cout1,2	Cin1,2	R1	C7
RTL8111H/RTL8107E	LDO	X	X	X	O	O
RTL8111HS/RTL8107ES	SWR	O	O	O	X	O
RTL8111H/RTL8107E	External	X	X	X	X	X
LMK41	LDO	X	X	X	R3101	C3101



25MHz XTAL

Change LAN PN to SC50H01259



LAN and Transformer Config:

LAN/Transformer	
RTL8111H 1000M 071.8111H.0003	
1000M Transformer 068.IH219.3001	Main source
1000M Transformer 068.69241.3011	2nd source

Crystal 27MHz			
MAIN	HASONIC	82.30020.G71	78.15034.L1L
2ND	HARMONY	82.30020.D41	78.18034.1FL

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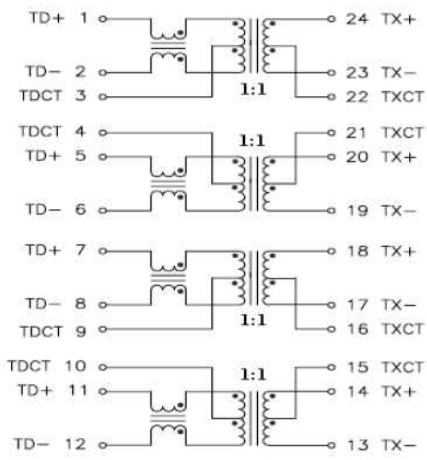
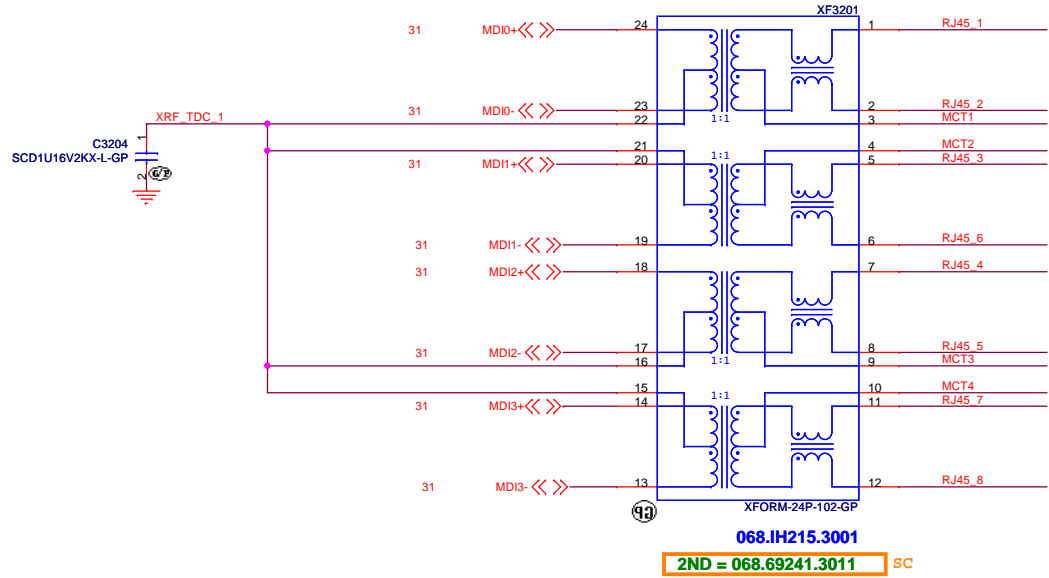
Title: **LAN RTL8111H**

Size A3 Document Number: **OSLO-SKLH** Rev: **SC**

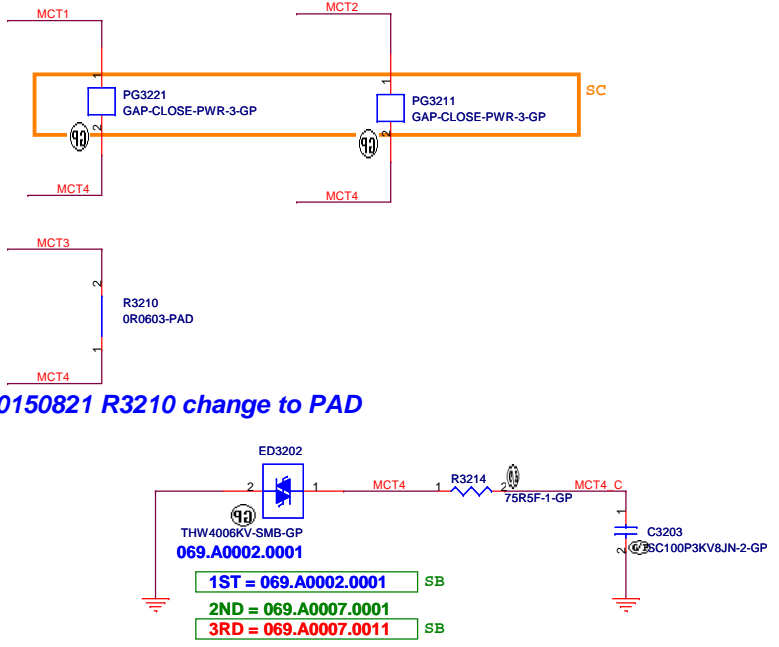
Date: Friday, August 28, 2015 Sheet 31 of 105

10/100M/1000M Lan Transformer

1000M Lan Transformer pin define



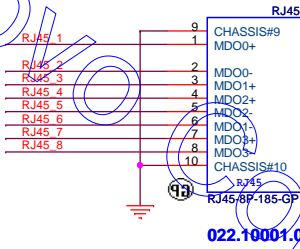
10/100/1000 LAN surge circuit
For test stuff



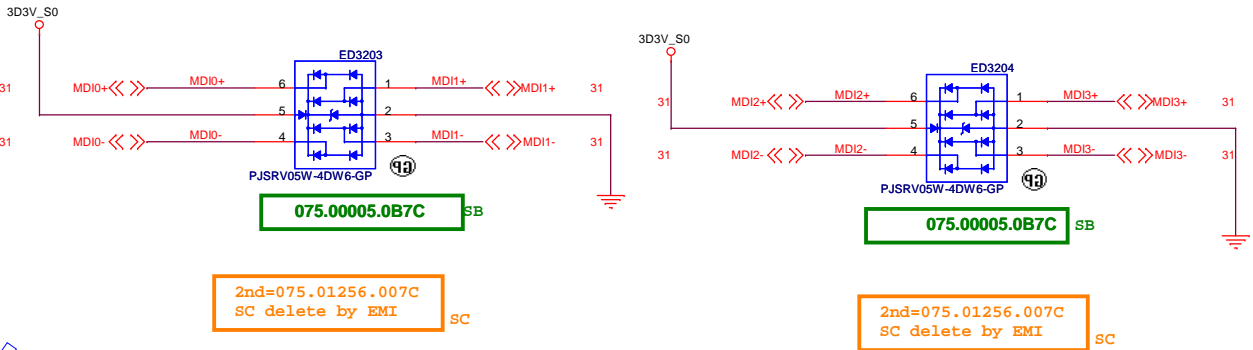
LAN and Transformer Config:

LAN/Transformer	
RTL8111GUL 1000M 20200540	
1000M Transformer 068.IH215.3001	Main source
1000M Transformer 068.69241.3011	2nd source
1000M Transformer 68.69241.30C	3rd source Reserve

LAN Connector



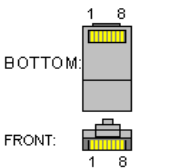
08/13 RJ45 22.10019.141 Change to 022.10001.00A1



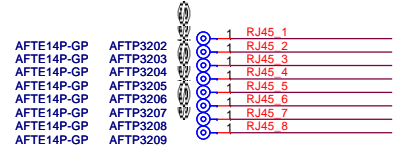
RJ45 Pin define

Pin	Description	10base-T	100Base-T	1000Base-T
1	Transmit Data+ or BiDirectional	TX+	TX+	BI_DA+
2	Transmit Data- or BiDirectional	TX-	TX-	BI_DA-
3	Receive Data+ or BiDirectional	RX+	RX+	BI_DB+
4	Not connected or BiDirectional	n/c	n/c	BI_DC+
5	Not connected or BiDirectional	n/c	n/c	BI_DC-
6	Receive Data- or BiDirectional	RX-	RX-	BI_DB-
7	Not connected or BiDirectional	n/c	n/c	BI_DD+
8	Not connected or BiDirectional	n/c	n/c	BI_DD-

The connector is 8 pin RJ45 (8P8C) male



The associated connector is 8 pin RJ45 (8P8C) female



AZ&NON AZ

Function LOCATION	AZ	NON AZ
ED3102	DY	ASM
R3114	DY	ASM
ED3103	ASM	DY
ED3104	ASM	DY
ED3105	ASM	DY
ED3106	ASM	DY
ED3107	ASM	DY
ED3108	ASM	DY
R3112	ASM	DY
R3115	ASM	DY
R3116	ASM	DY
R3117	ASM	DY
R3118	ASM	DY
R3119	ASM	DY
R3120	ASM	DY

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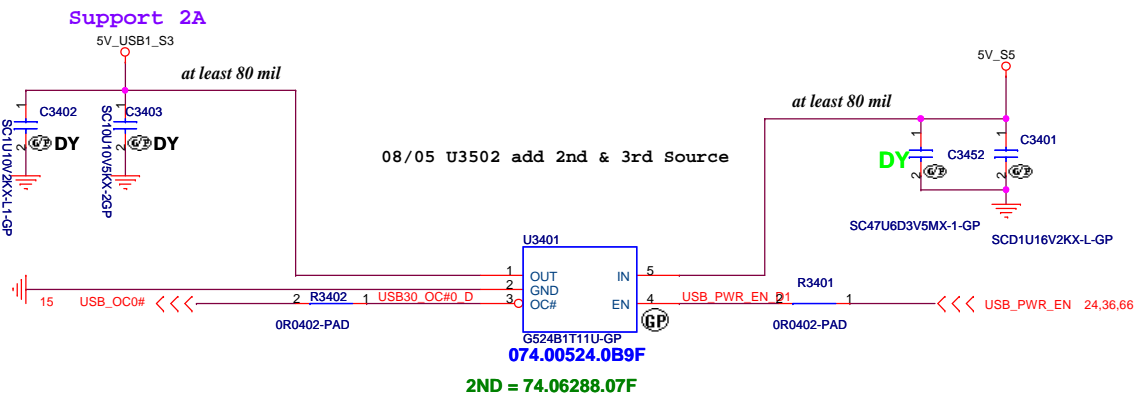
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3

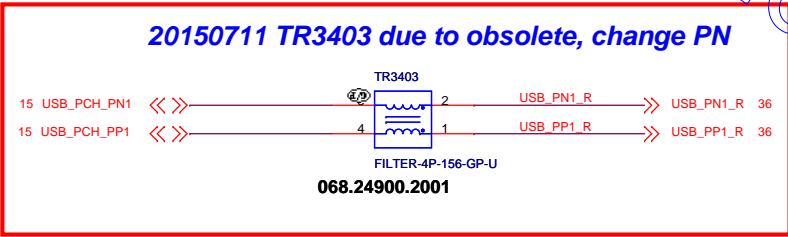
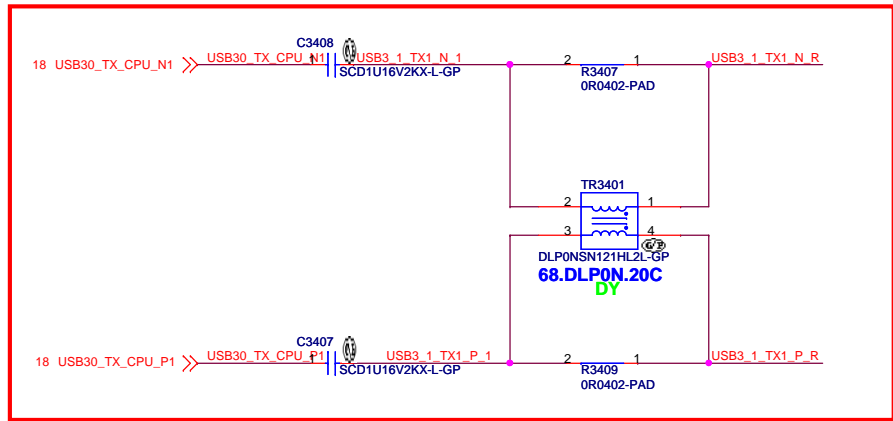
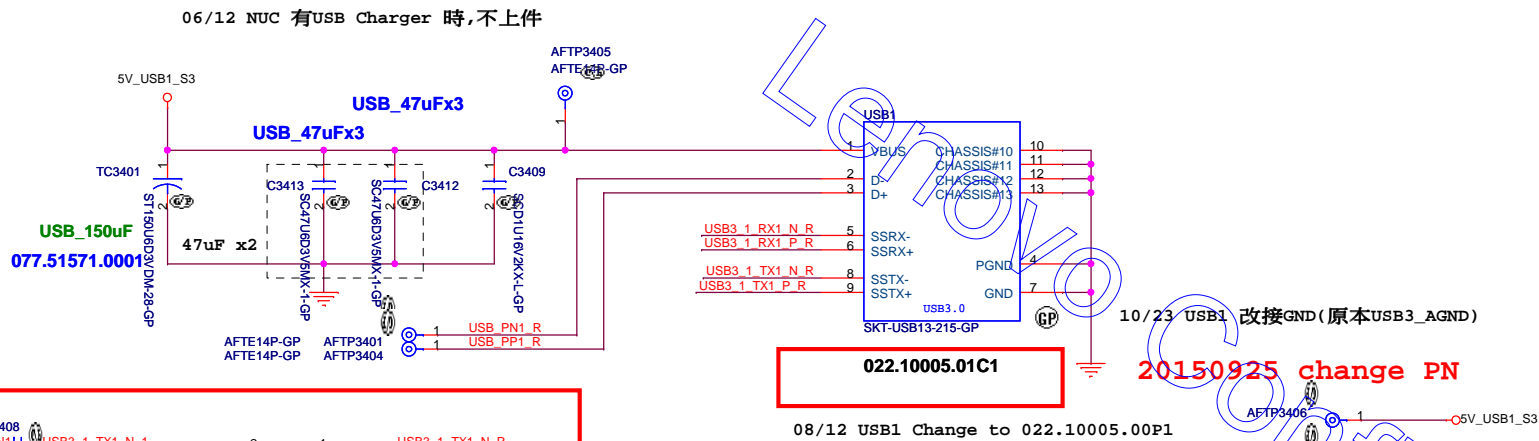
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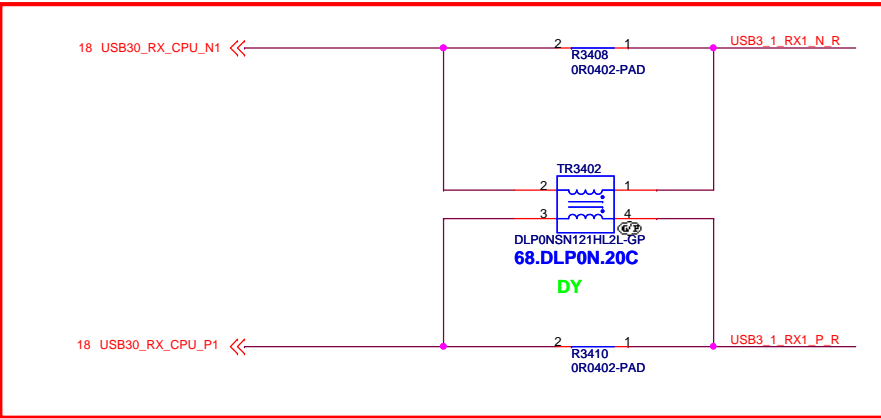


USB 3.0 Connector
Pin definition

1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

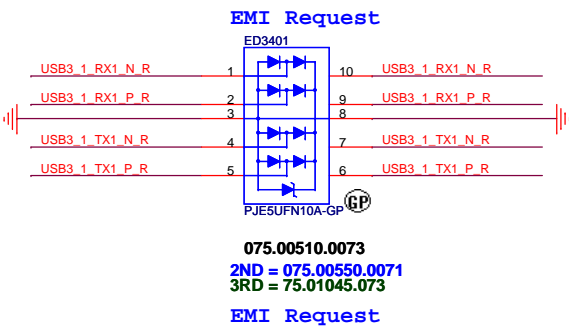


20150527 layout swap



20150825 R3407 R3408 R3409 R3410 change to PAD

20150825 install TR3403

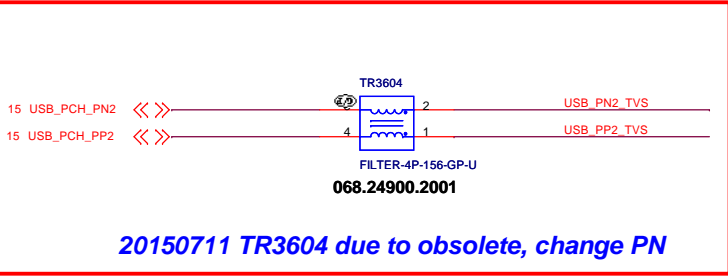
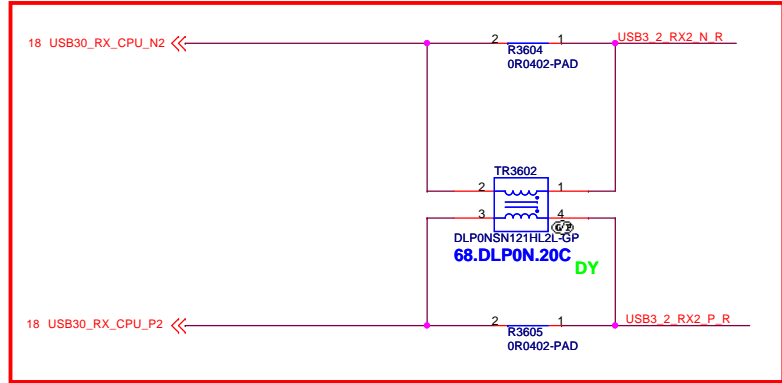
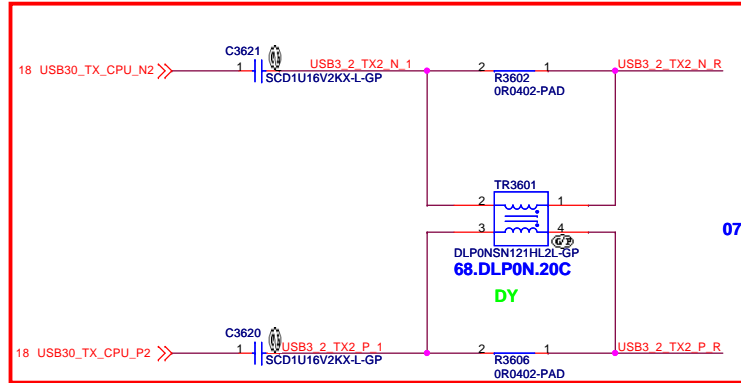
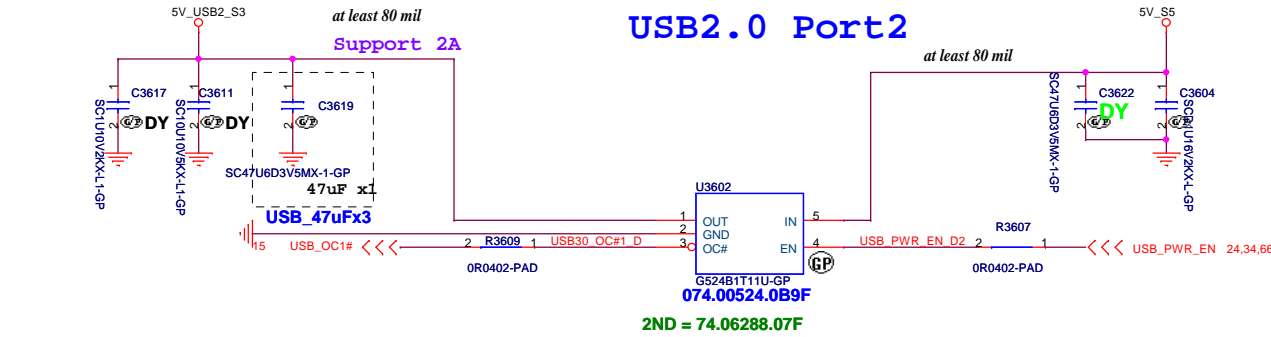


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<div>Title</div> <div>(Reserved)</div>			
<div>Size</div> <div>A3</div>	<div>Document Number</div> <div>OSLO-SKLH</div>		<div>Rev</div> <div>SC</div>
<div>Date:</div> <div>Saturday, July 11, 2015</div>		<div>Sheet</div> <div>35</div>	<div>of</div> <div>105</div>

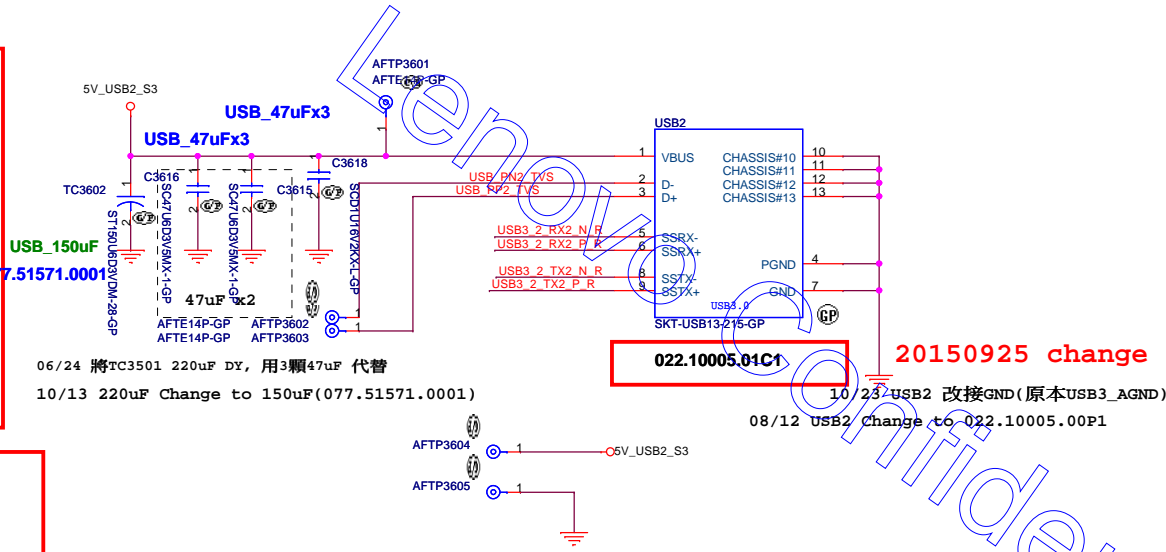


20150711 TR3604 due to obsolete, change PN

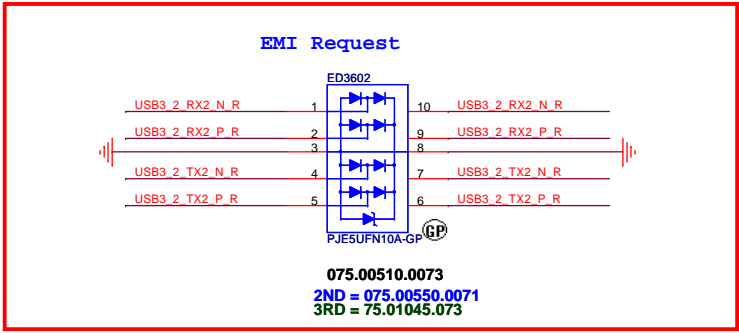
20150527 layout swap

WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR

20150825 install TR3604

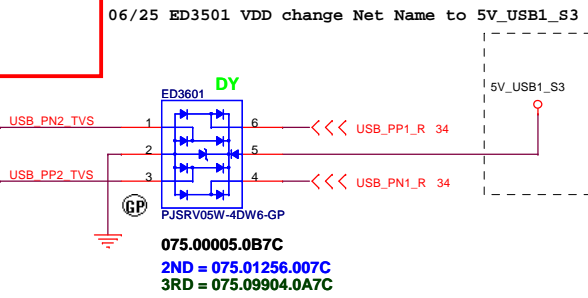


20150825 R3602 R3604 R3605 R3606 change to PAD



08/18 ED3501 USB_PP2 Change to USB_PP2_TVS
USB_PN2 Change to USB_PN2_TVS
USB_PP1_CHG Change to USB_PP1_R
USB_PN1_CHG Change to USB_PN1_R

08/19 ED3501 USB_PN1_R 與 USB_PP1_R SWAP
USB_PP2_TVS 與 USB_PN2_TVS SWAP



6/17 ED3501 Change Part Number to 75.09904.07C
與 ED3602 合併,共用一顆ESD

5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

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20150706 remove 3D camera

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D																								
C																								
B																								
A																								
5					4					3					2					1				

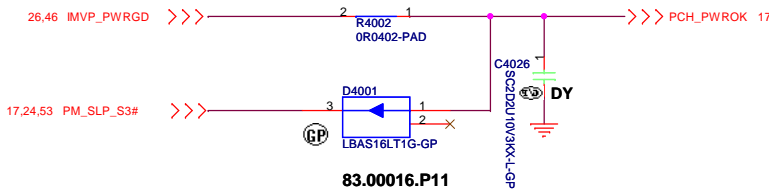
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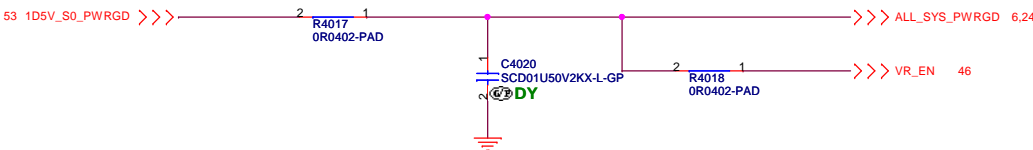
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Title <div>(Reserved)</div>				
Size <div>A</div>	Document Number <div>OSLO-SKLH</div>			Rev <div>SC</div>
Date: Saturday, July 11, 2015			Sheet 39 of 105	

Power Sequence

20150828 reserve C4026
20151013 R4002 R4006 R4008 R4017 change to PAD



20150716 change D4001 PN

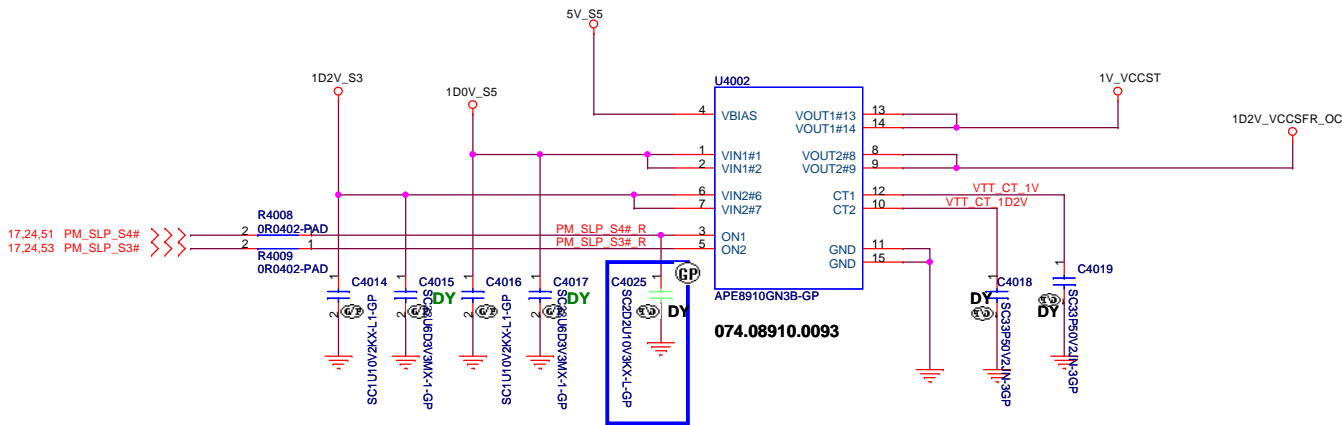
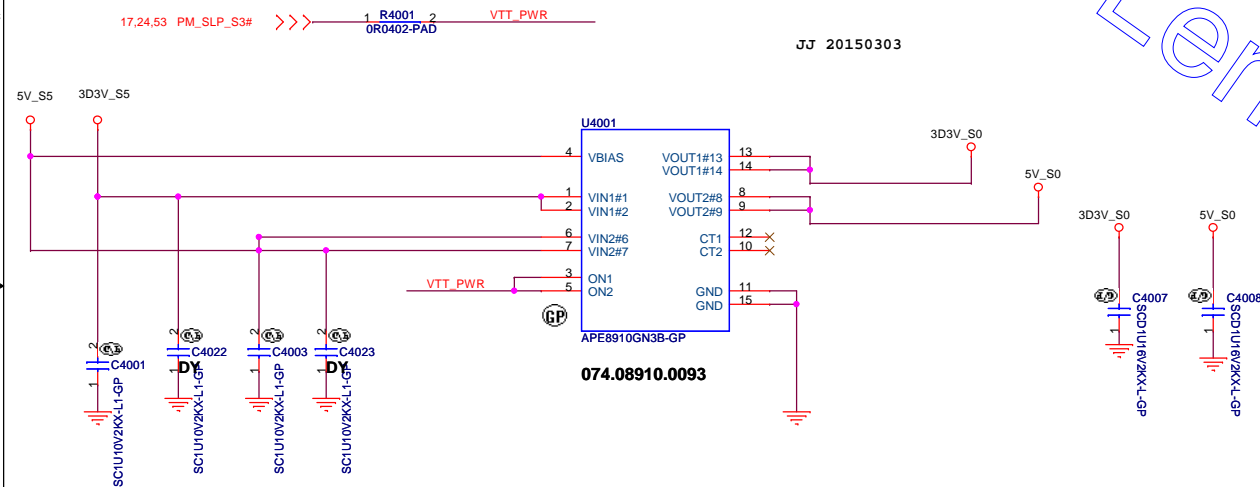


20150828 R4009 R4018 change to PAD

20150703 reserve C4025

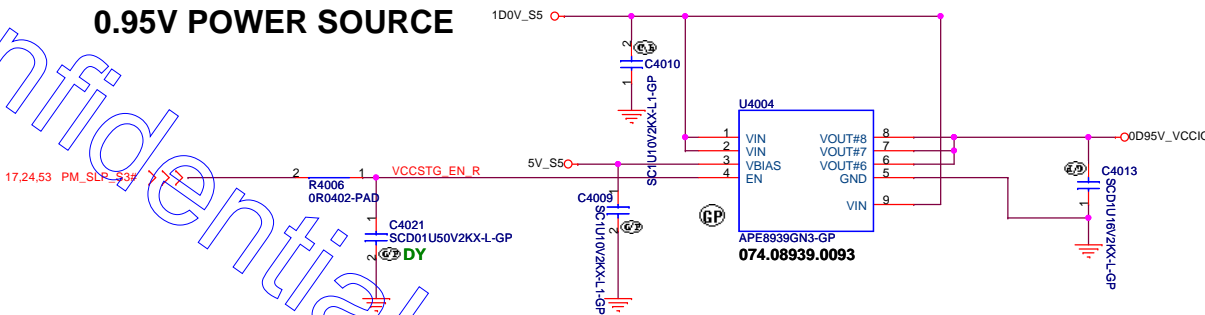
ANNIE Run Power

20150601 change U4001 U4002 PN

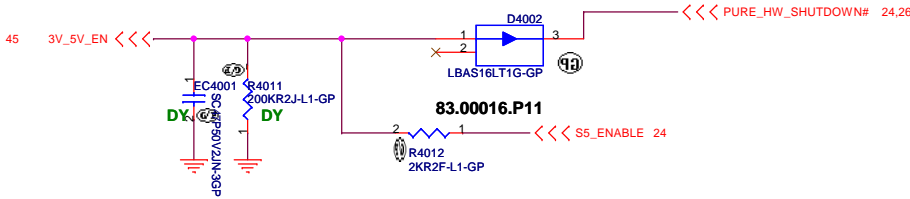


20150703 reserve C4025

0.95V POWER SOURCE



20150716 change D4002 PN



20150601 remove 1D8V

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Title (Reserved)DS3			
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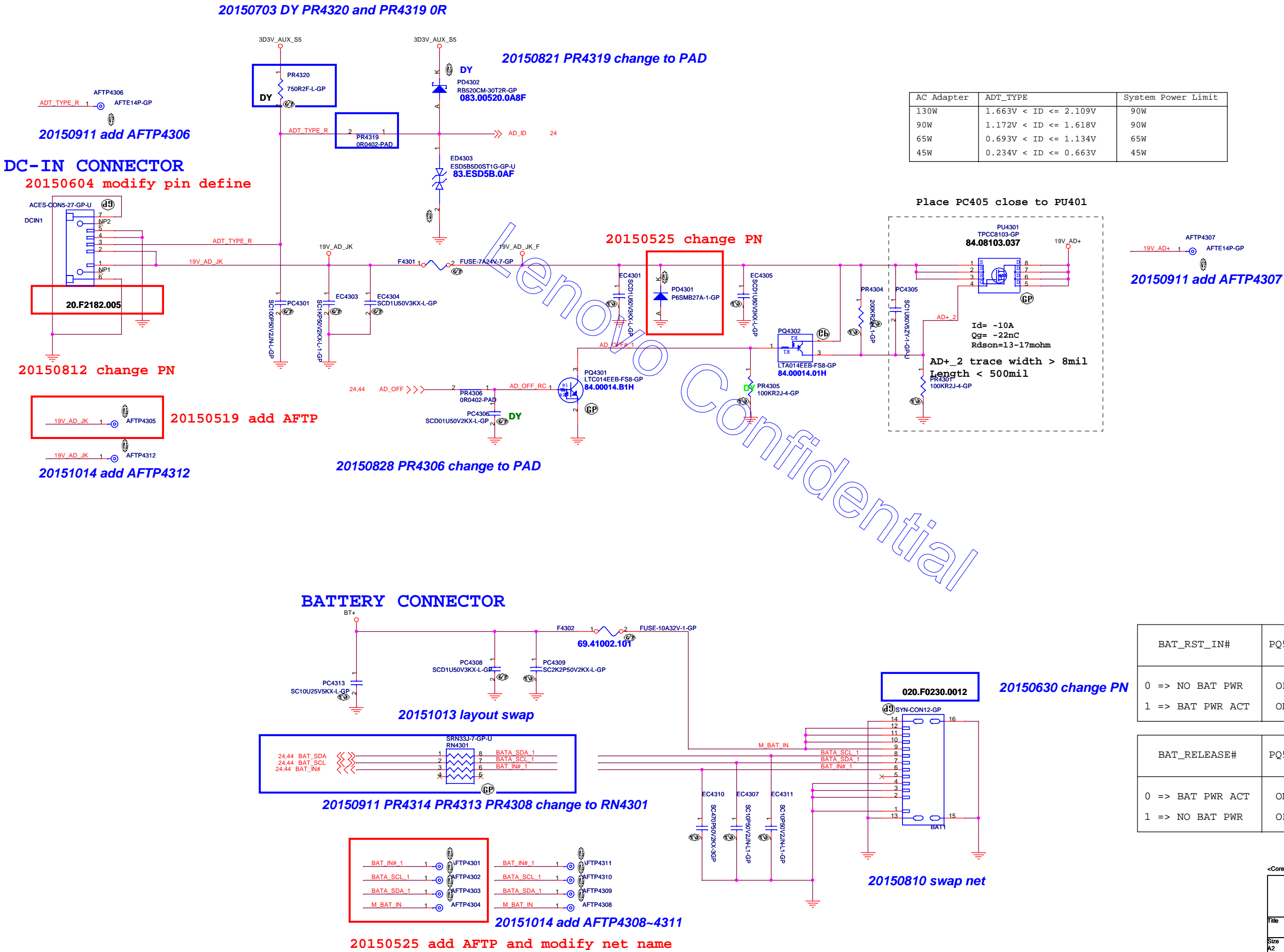
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B				B
A				A
5	4	3	2	1

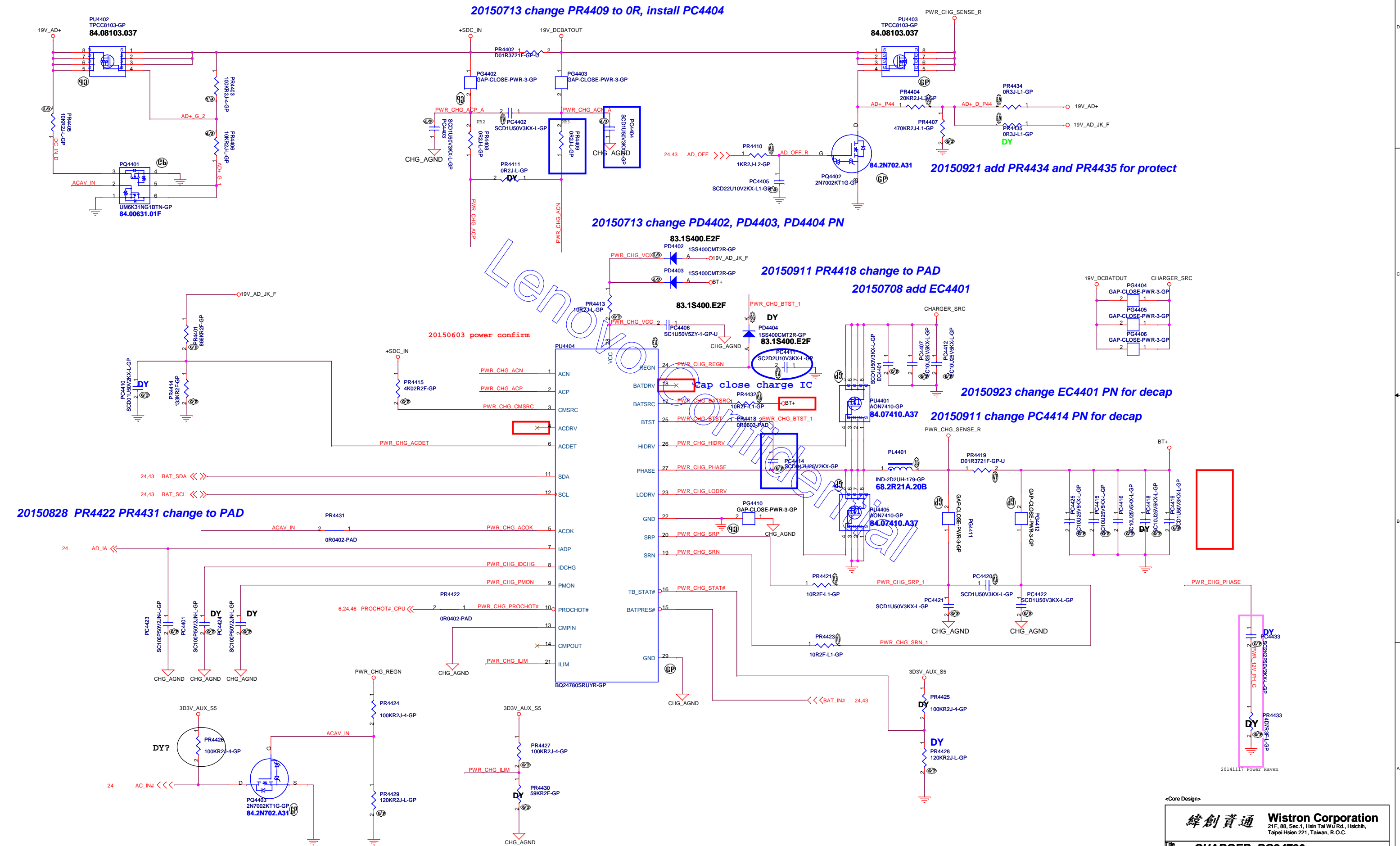
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Main Func = DC-IN CONN
Main Func = BATT CONN





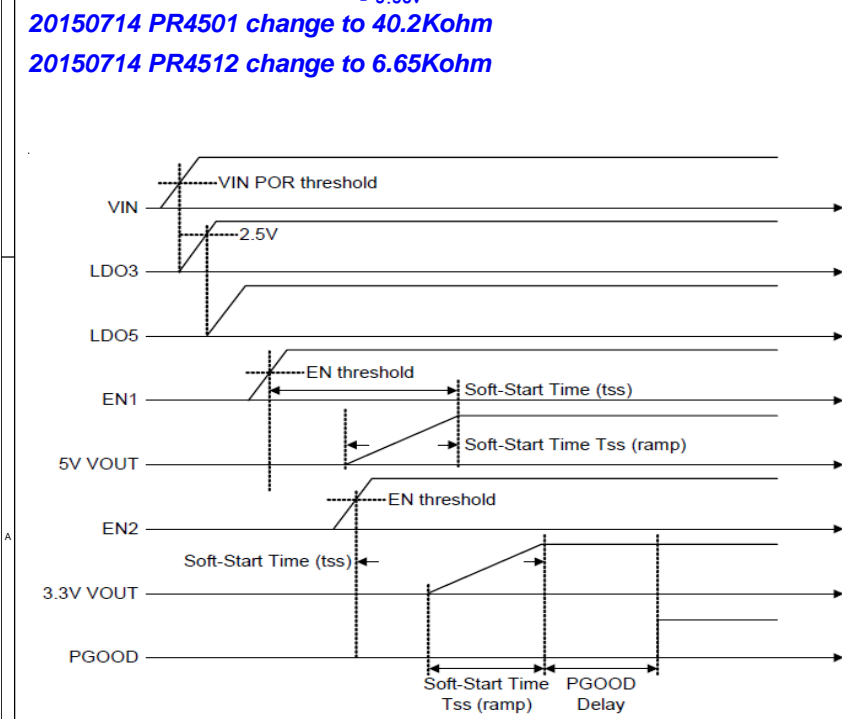
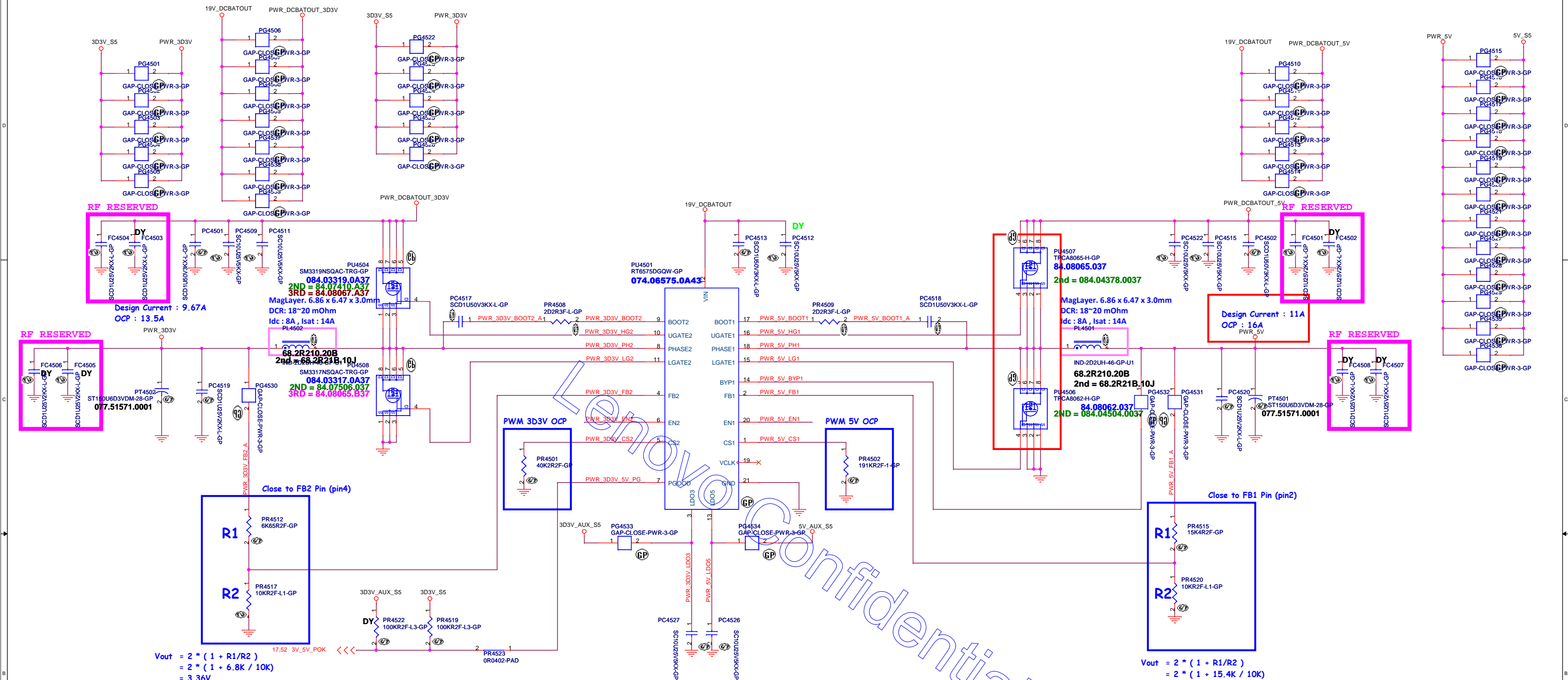
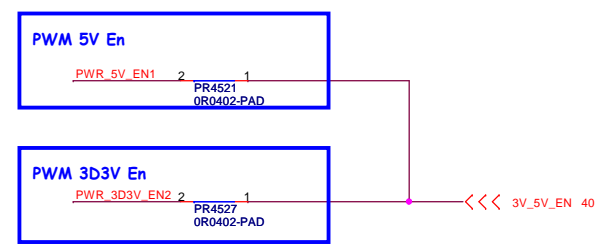
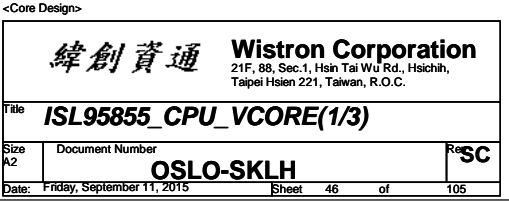


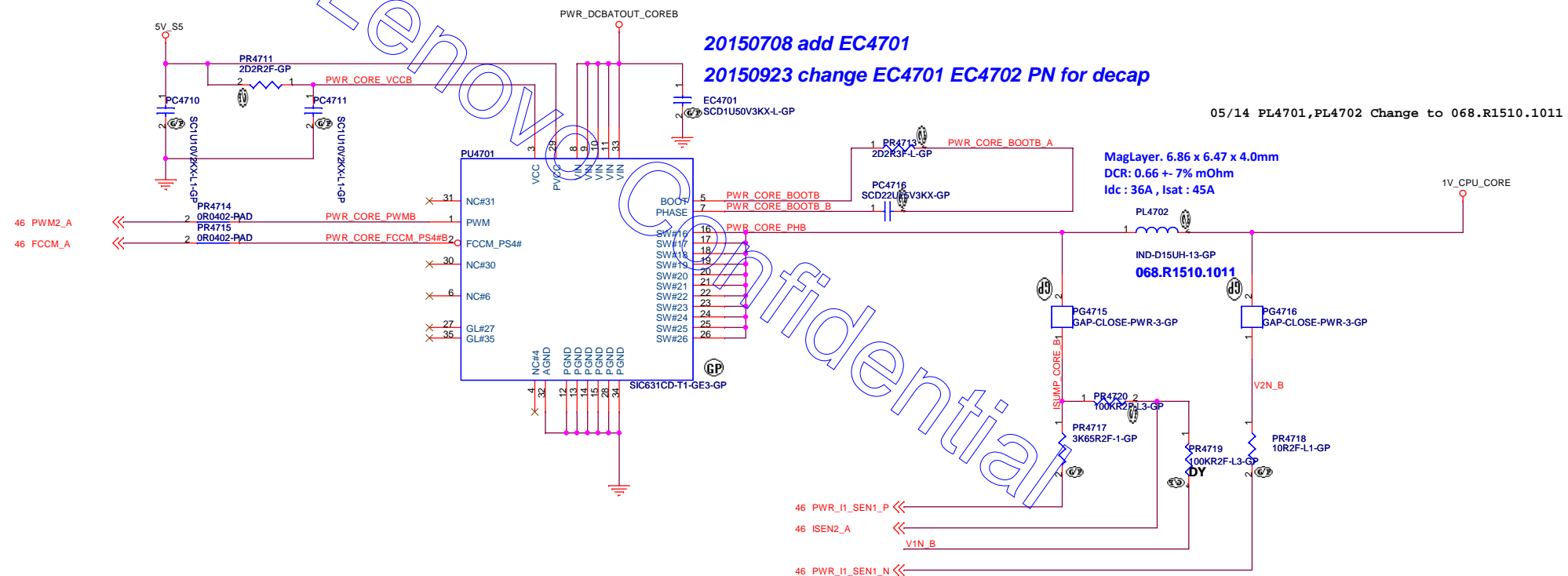
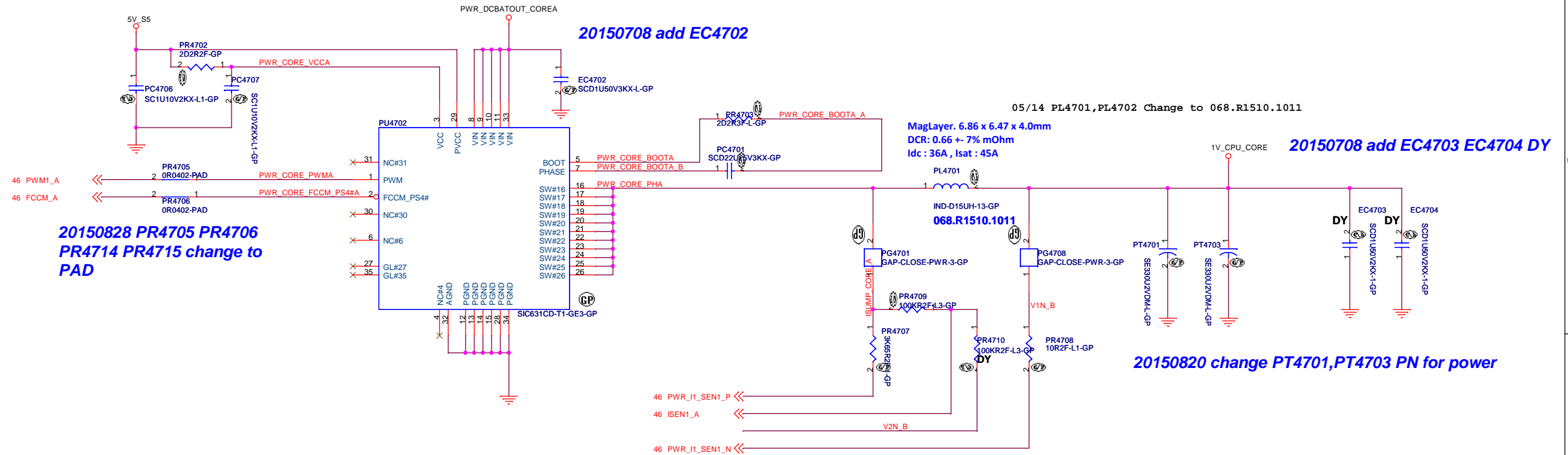
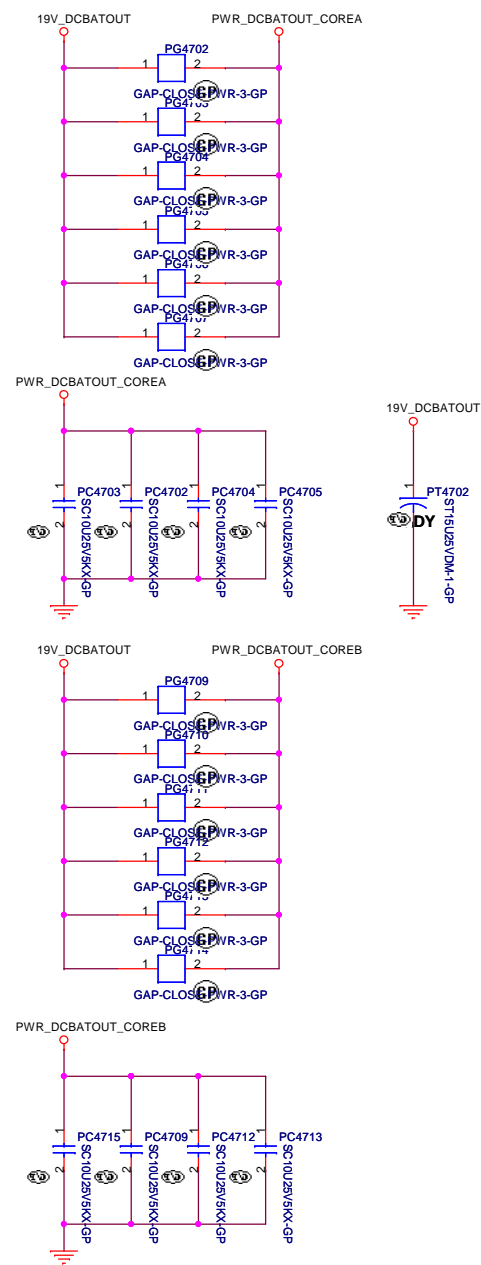
Figure 6. RT6575B Timing



Vin POR threshold , Rising :4.6 V ; Failing : 3.7 V
 EN threshold Logic-High : 1.6 V
 EN threshold Logic-Low : 0.4 V

20150828 PR4521 PR4523 PR4527 change to PAD





20150708 add EC4801

20150824 add EC4805
20150923 change EC4801 EC4802 EC4805 EC4806 PN for decap

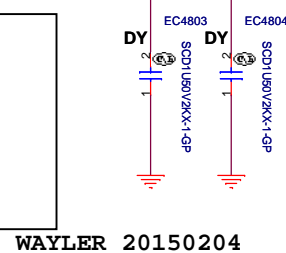
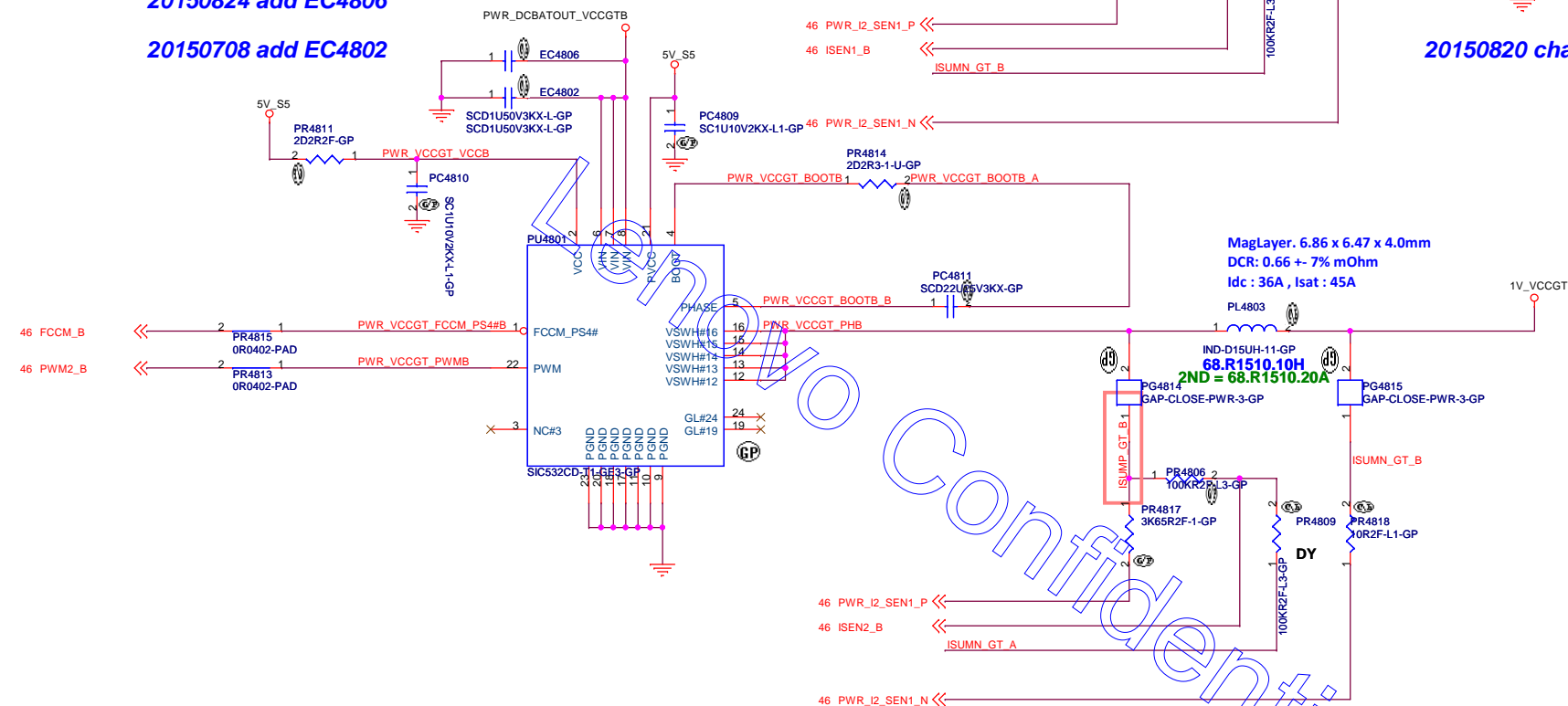
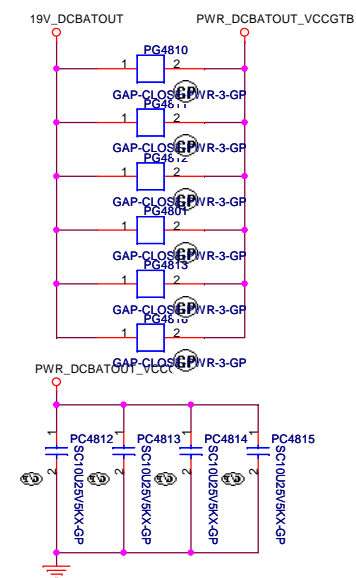
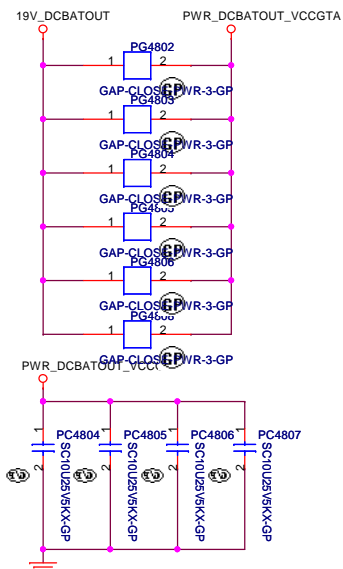
20150708 add EC4803 EC4804 DY

20150828 PR4801 PR4805 PR4815
PR4813 change to PAD

20150824 add EC4806

20150708 add EC4802

20150820 change PT4801,PT4803 PN for power



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File			SIC631CD_CPU_VCORE(2/3)
Size	Document Number	Rev	SC
A2			
Date	Wednesday, September 23, 2015	Sheet	48 of 105

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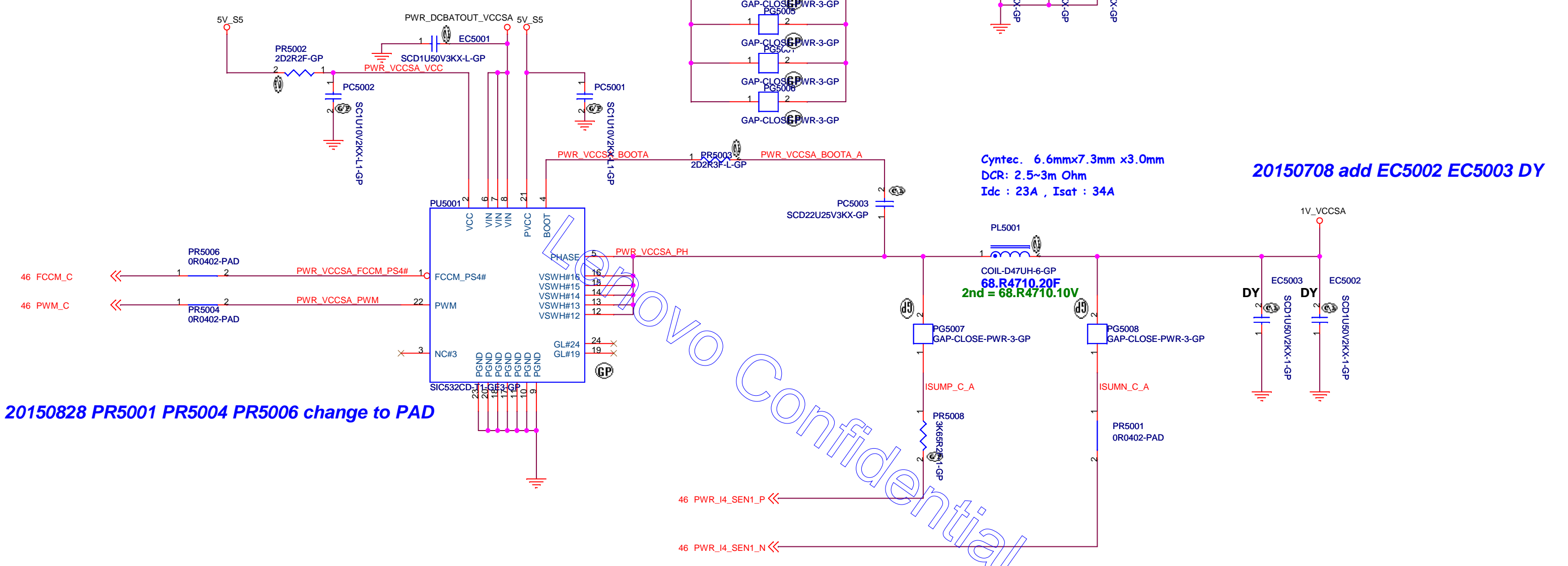
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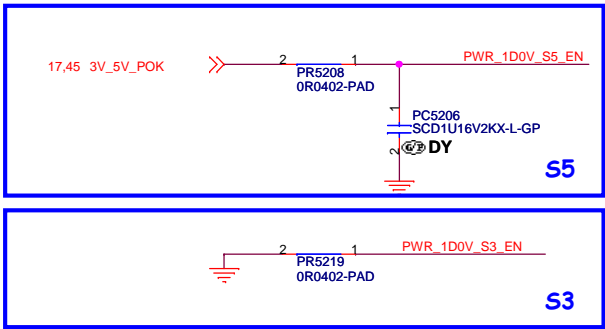
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20150923 change EC5001 PN for decap
20150708 add EC5001

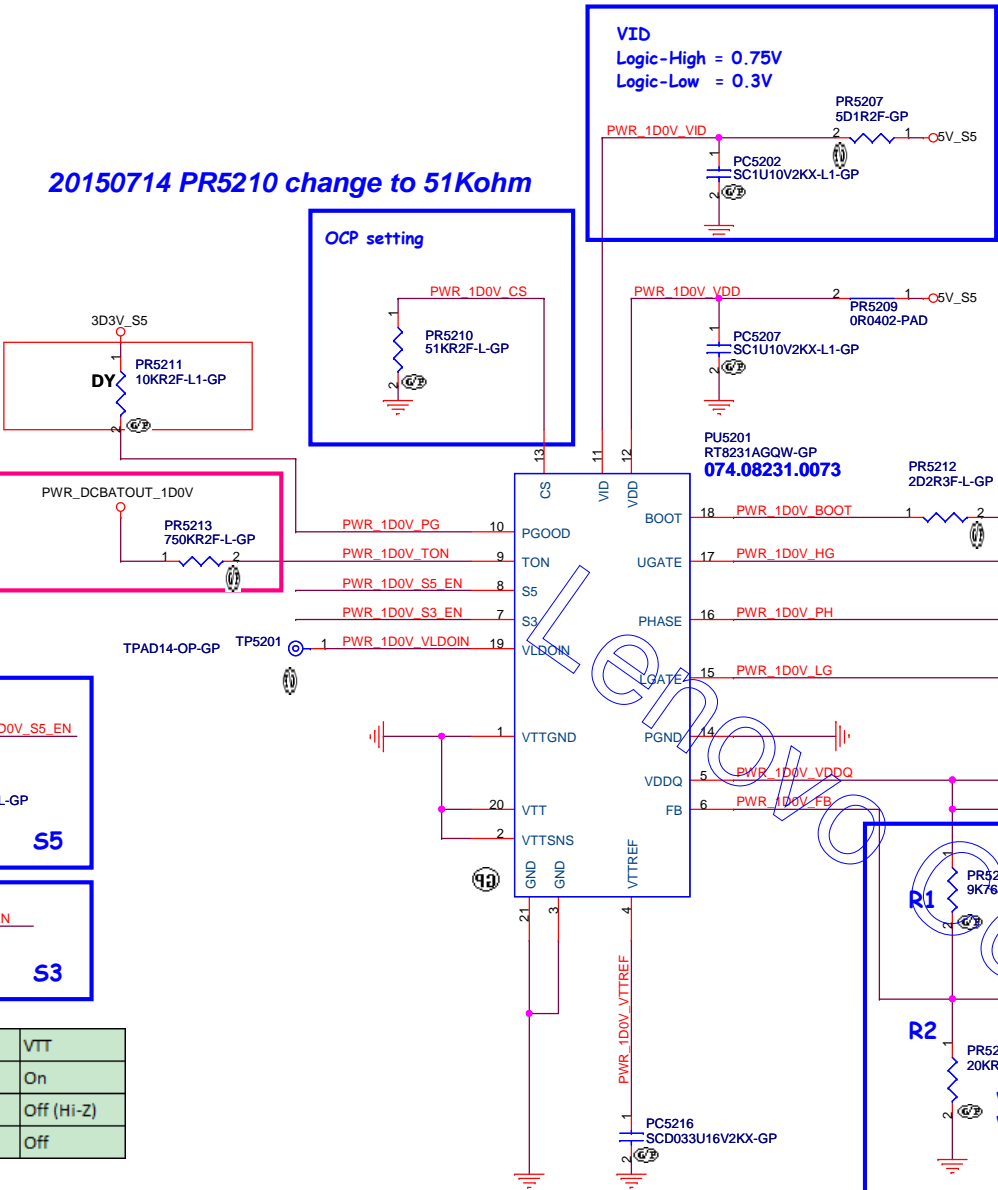


20150828 PR5208 PR5209 PR5219
change to PAD



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

20150714 PR5210 change to 51Kohm

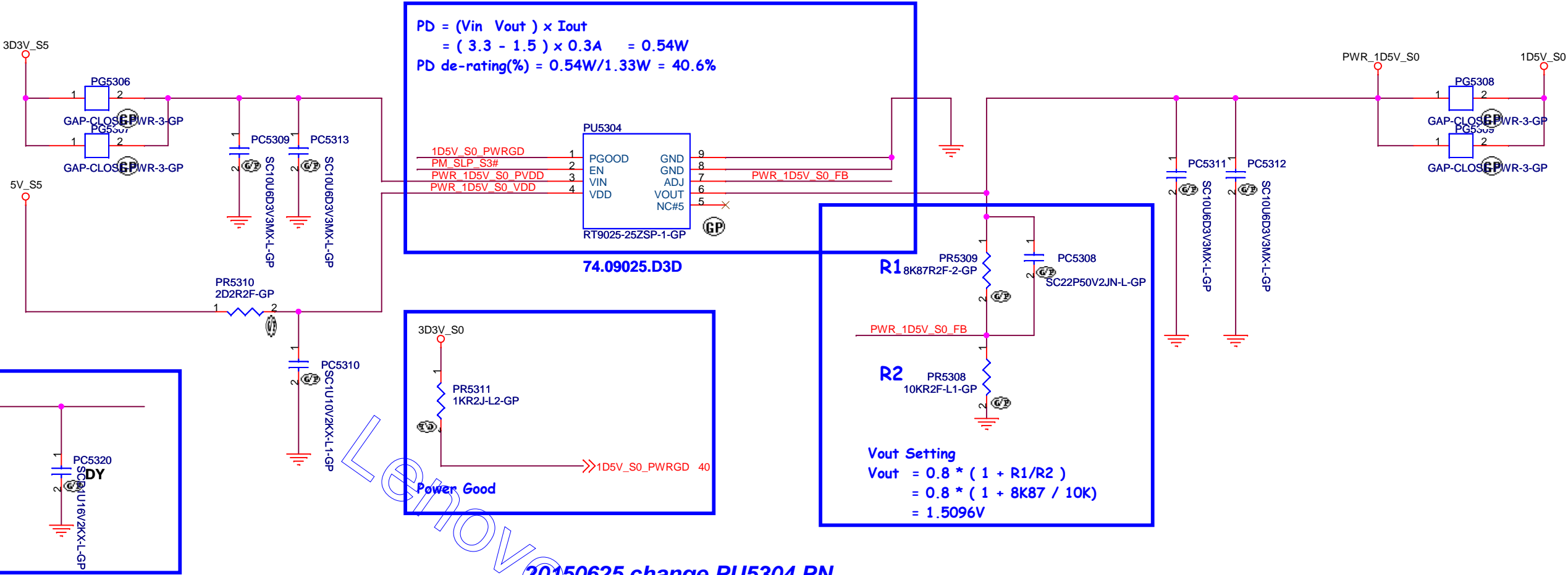


VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note. Vref can only be changed from
0.675v to 0.75v after power-on

Vout Setting
$$V_{out} = V_{ref} * (1 + R1/R2)$$
$$= 0.675 * (1 + 9.76K / 20K)$$
$$= 1.004 V$$

<Core Design>

1D5V_S0



20150625 change PU5304 PN

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D				D
C				C
B				B
A				A
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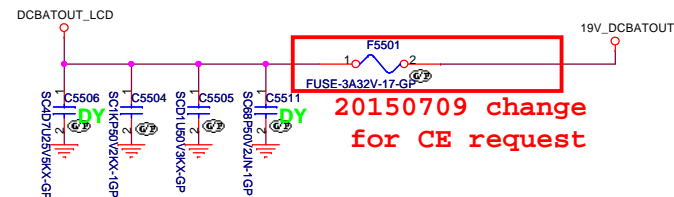
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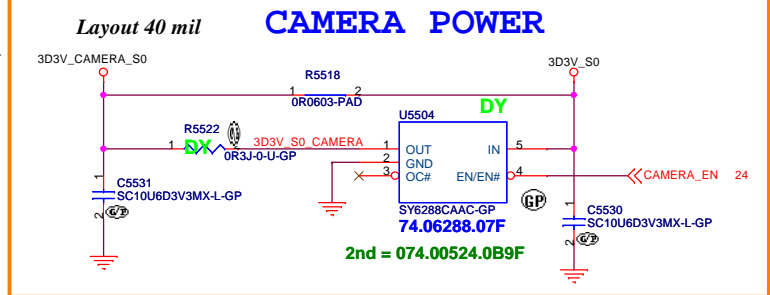
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SSID = VIDEO

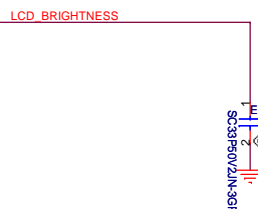
INVERTER POWER



CAMERA POWER



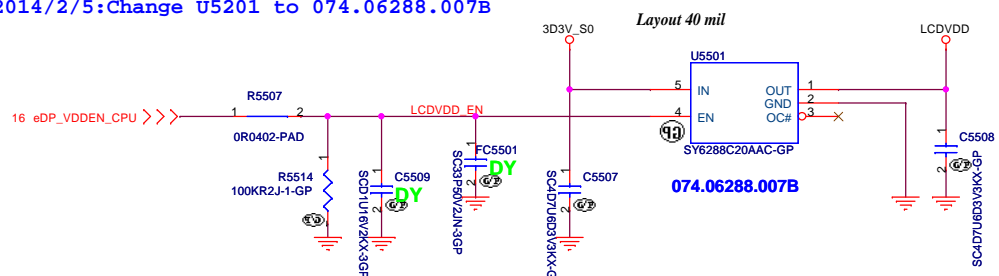
Close to eDP connector



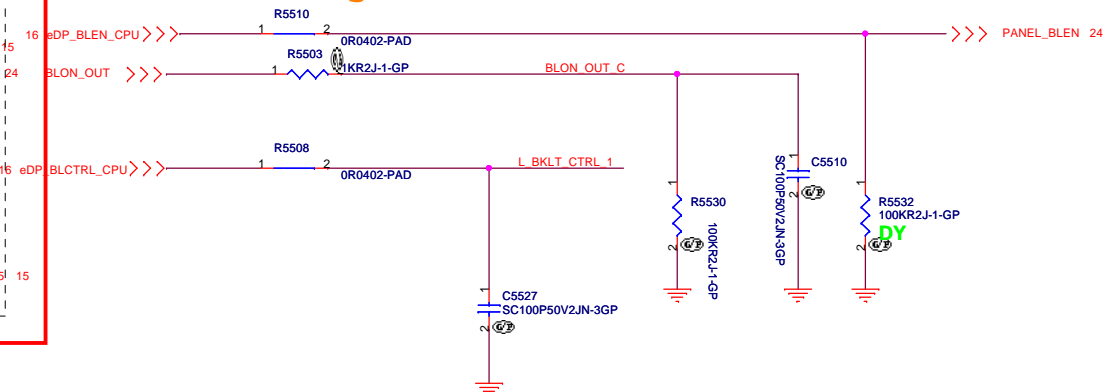
SSID = VIDEO

LCD POWER (Do Not use SW 74.09724.09F)

2014/2/5:Change U5201 to 074.06288.007B

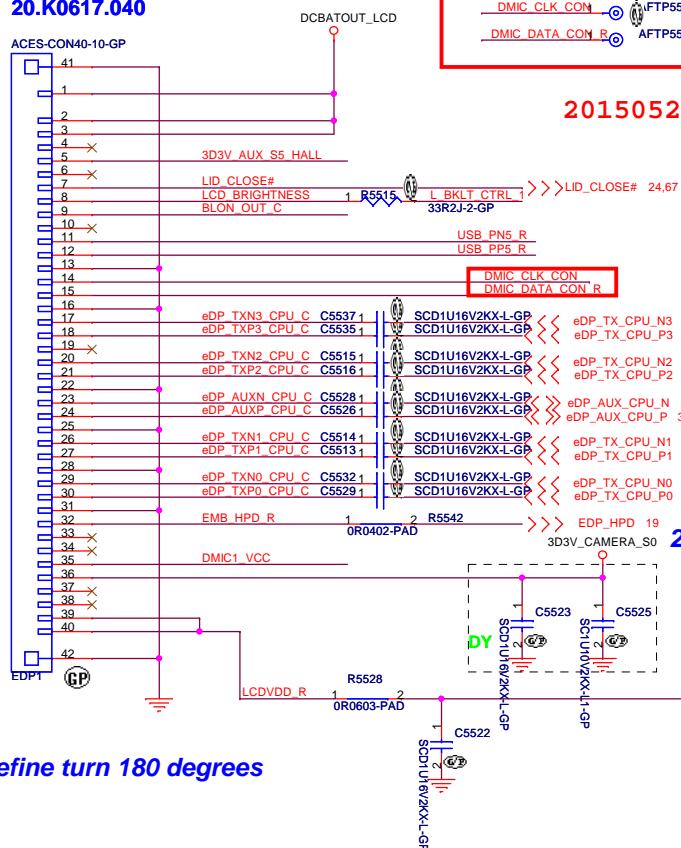


Panel BL brightness/Power En/BL En



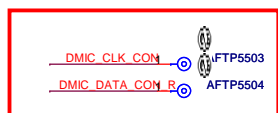
eDP connector

2nd = 20.K0568.040
20.K0617.040



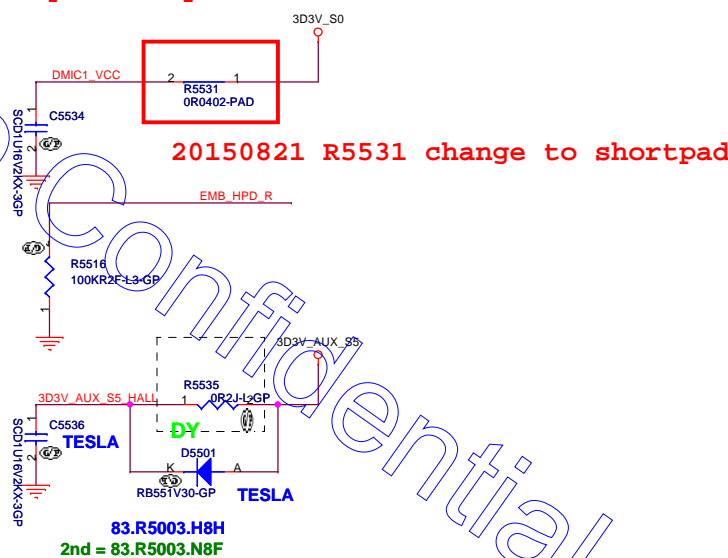
20150519 add AFTP

20150519 add AFTP



20150525 add AFTP

20150601 layout swap



Lid

DMIC

4 lane EDP
eDP Panel

20150911 remove 3D_DETECT

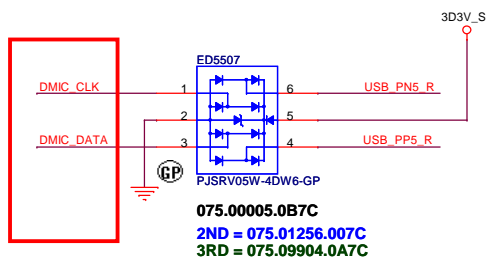
08/18 add C5523(0.1uF), C5525(1uF)

20151006 EDP pin define turn 180 degrees

20150911 add AFTP5502

20150603 layout swap

CCD for ESD Request



20150827 R5504 R5505 33ohm, EC5501 EC5503 33P for E MI

20150520 change from page38 to 55

<Core Design>

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Title LCD&CAM&DMC&Touch
Size A2 Document Number OSLO-SKLH Rev SC
Date: Tuesday, October 06, 2015 Sheet 55 of 105

5

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Size A	Document Number OSLO-SKLH	Rev SC
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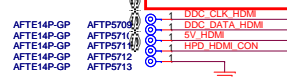
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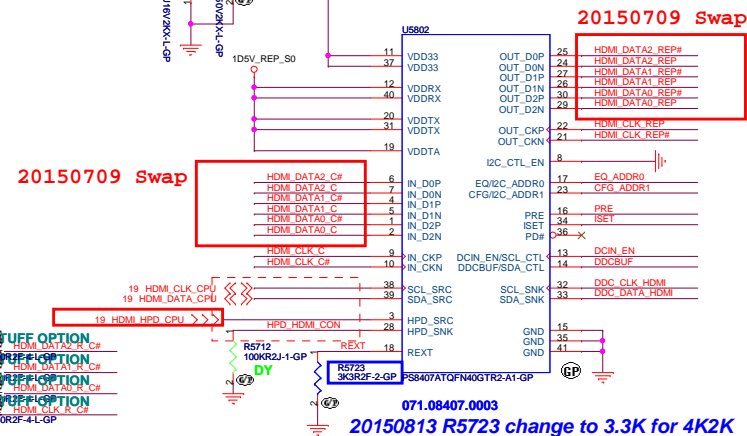
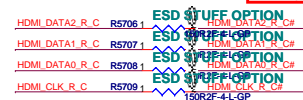
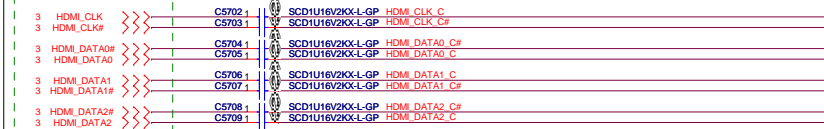
SSID = VIDEO

20150710 delete AFTP



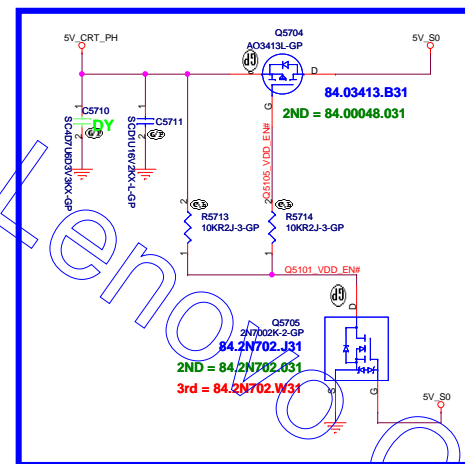
Close to HDMI Connector

HDMI Passive Level Shifter

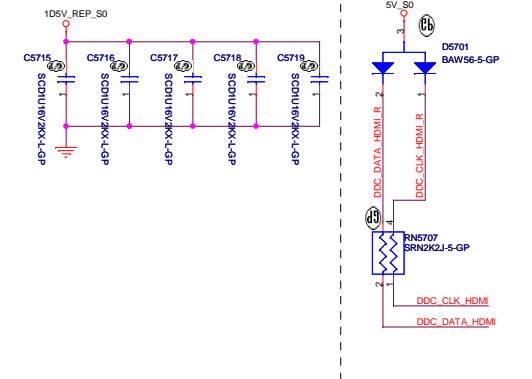


HDMI DDC Passive Level Shifter

20150520 delete DDC passive level shifter

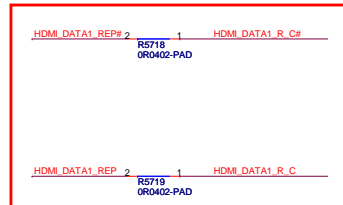
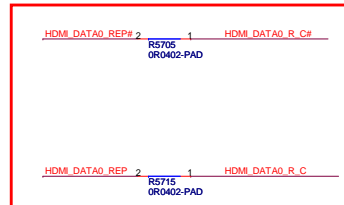


07/02 Change Part Number 84.07002.I31(禁用) to 84.2N702.J31

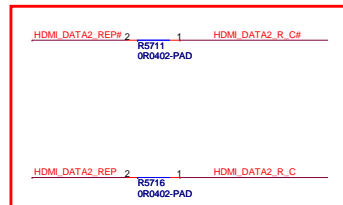
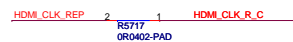


Pin	Pin 定義
1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2-
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1-
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0-
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock-
13	CEC
14	Reserved (N.C. on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect

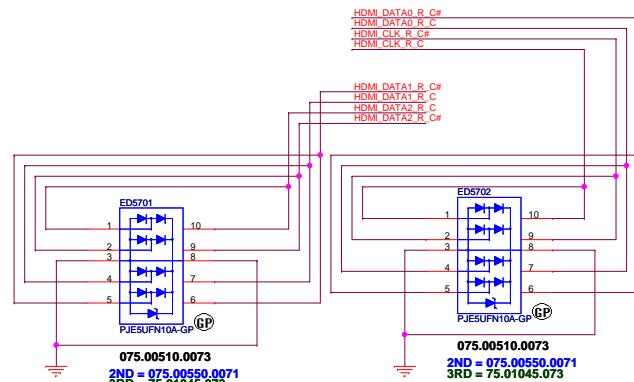
20150821 R5721 R5722 R5705 R5715 R5718 R5719 R5710 R5717 R5711 R5716 change to PAD



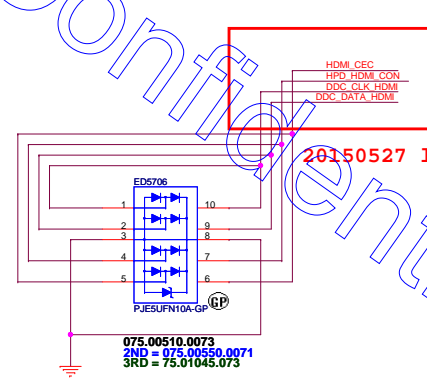
20150602 remove TR5701~TR5704



20150527 layout swap



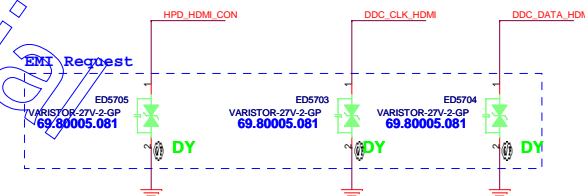
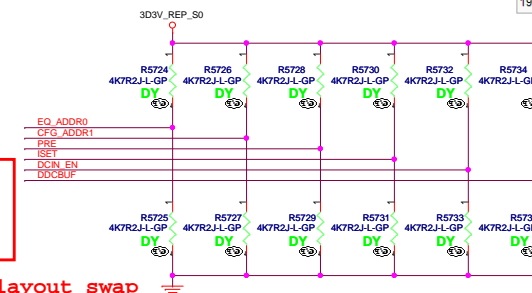
10/15 ED5701,ED5702,ED5706 Change Part number to 75.00524.073



08/18 add ED5706

08/19 HPD_HDMI_CON & DDC_CLK_HDMI SWAP

20150527 layout swap



20150520 change PN

HDMI A type pin define
(Total: 19pin)

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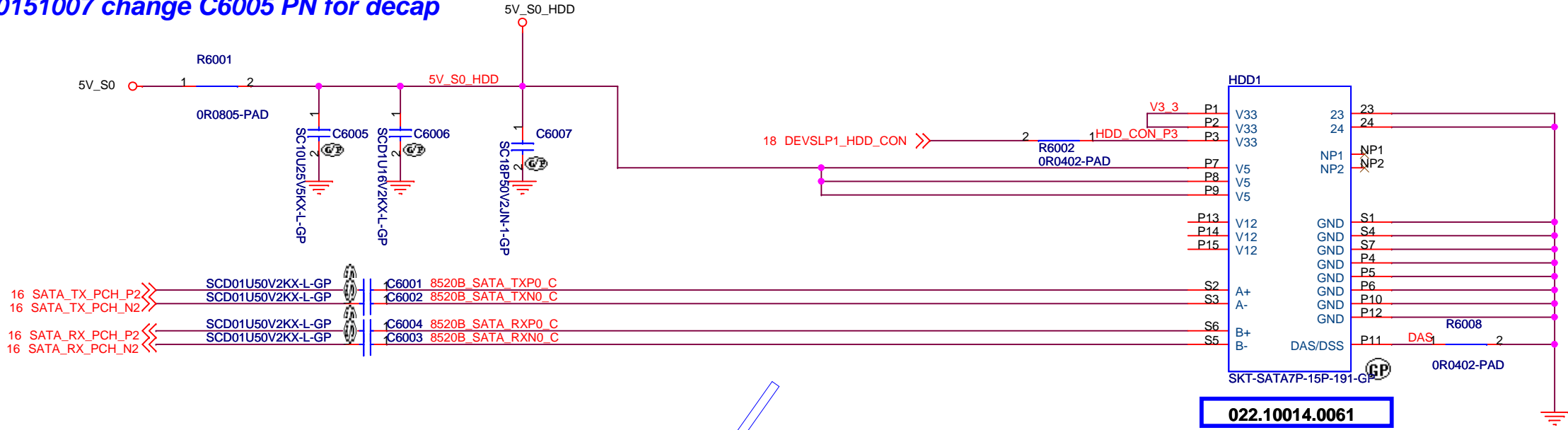
Size A	Document Number OSLO-SKLH	Rev SC
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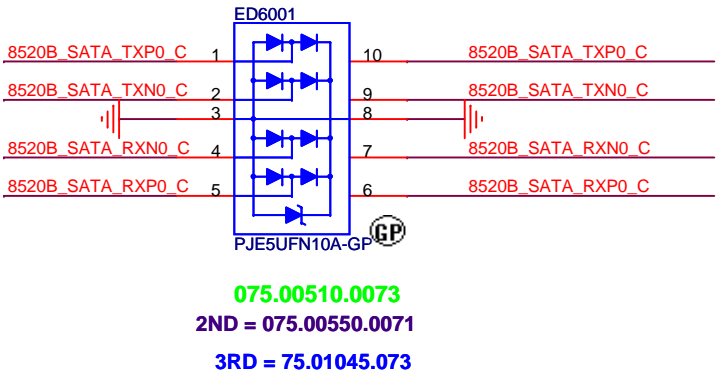
SSID = SATA

20151007 change C6005 PN for decap

20150821 R6002 R6001 change to PAD



20150812 change PN



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SSID = Wireless

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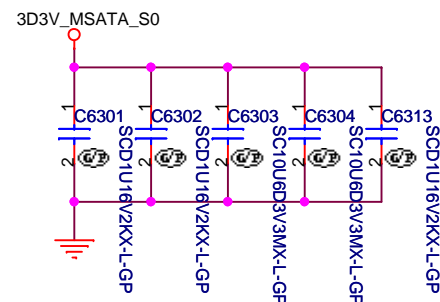
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Title			
(Reserved)WWAN			
Size A	Document Number		Rev
	OSLO-SKLH		SC
Date: Saturday, July 11, 2015		Sheet 62	of 105

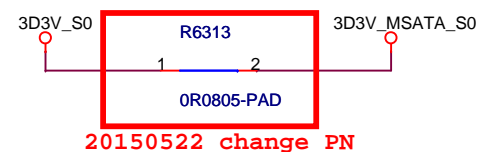
SSID = m-SATA

Mini Card Connector (NGFF m-SATA)

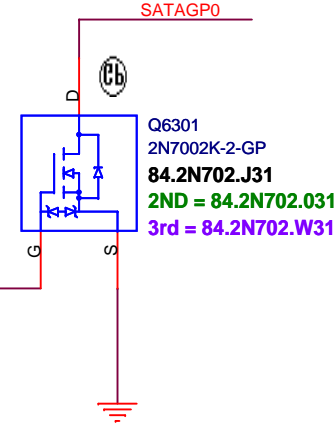
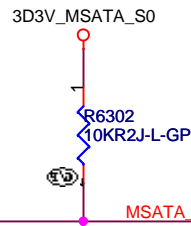
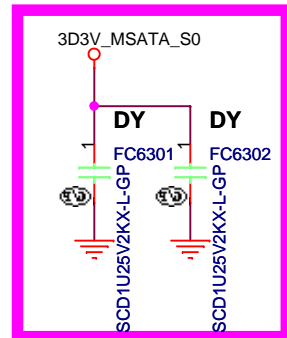
20150825 install C6313 for EMI



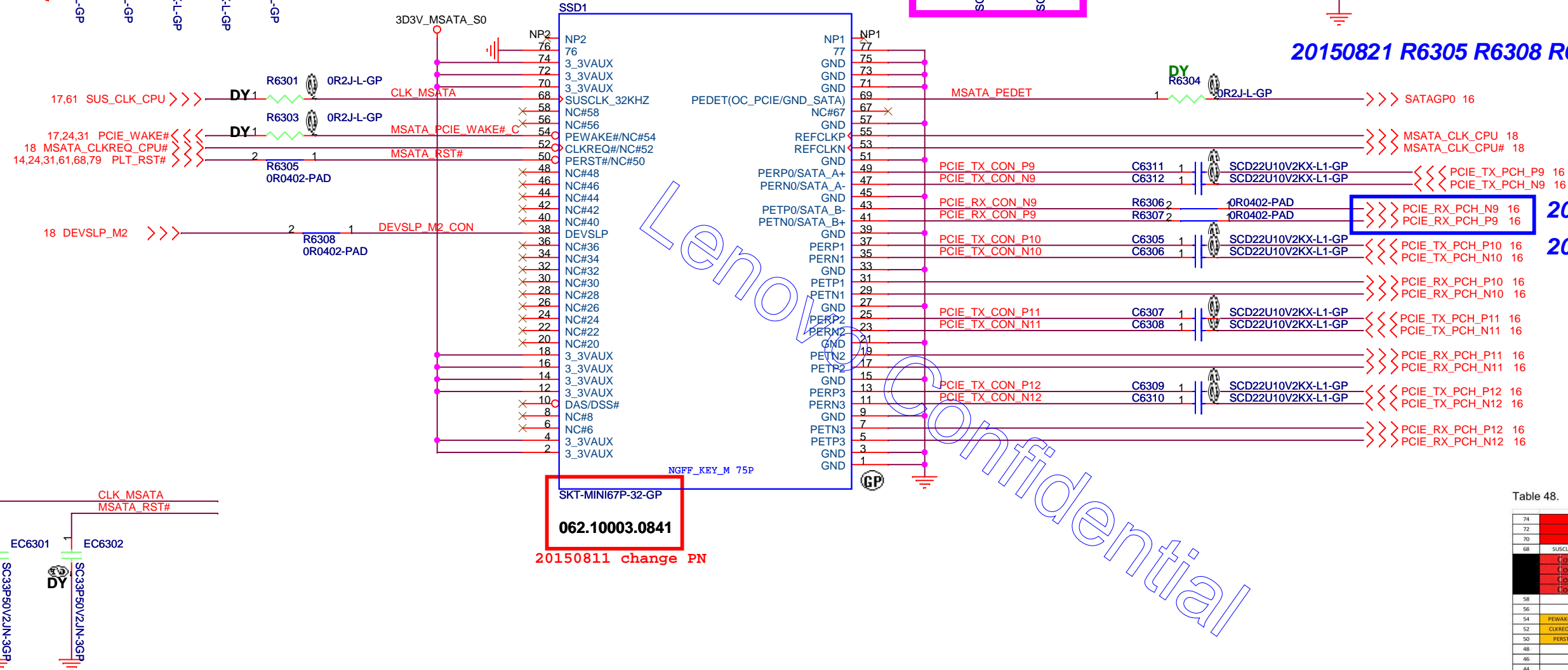
20150821 R6313 change to PAD



RF RESERVED



20150821 R6305 R6308 R6306 R6307 change to PAD



20150711 add 0R
20150714 swap P,N

Table 34-5. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

Notes:

- Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
- Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
- Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
- Design Constraints, Required: Refer to the Chapter 3, "General Differential Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	75	GND
72	3.3V	73	GND
70	N/C	71	GND
68	SUSCLK(32KHz) (IOIO/3.3V)	69	PEDET (NC-PCIE/GND-SATA)
	Connector Key	67	N/C
	Connector Key		
	Connector Key		
	Connector Key		
	Connector Key		
58	N/C	57	GND
56	N/C	55	REFCLKP
54	PEWAKE# (VDDIO/3.3V) or N/C	53	REFCLKN
52	CLKREQ# (VDDIO/3.3V) or N/C	51	GND
50	PERST# (GND/3.3V) or N/C	49	PETp0/SATA-A+
48	N/C	47	PETn0/SATA-A-
46	N/C	45	GND
44	N/C	43	PERp0/SATA-B+
42	N/C	41	PERn0/SATA-B-
40	N/C	39	GND
38	DEVSLP (IO)	37	PETp1
36	N/C	35	PETn1
34	N/C	33	GND
32	N/C	31	PERp1
30	N/C	29	PERn1
28	N/C	27	GND
26	N/C	25	PETp2
24	N/C	23	PETn2
22	N/C	21	GND
20	N/C	19	PERp2
18	3.3V	17	PERn2
16	3.3V	15	GND
14	3.3V	13	PETp3
12	3.3V	11	PETn3
10	DAS/DSS# (VDDIO/LEDSP (IOIO/3.3V))	9	GND
8	N/C	7	PERp3
6	N/C	5	PERn3
4	3.3V	3	GND
2	3.3V	1	GND

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Title

SSD-NGFF

Size A3

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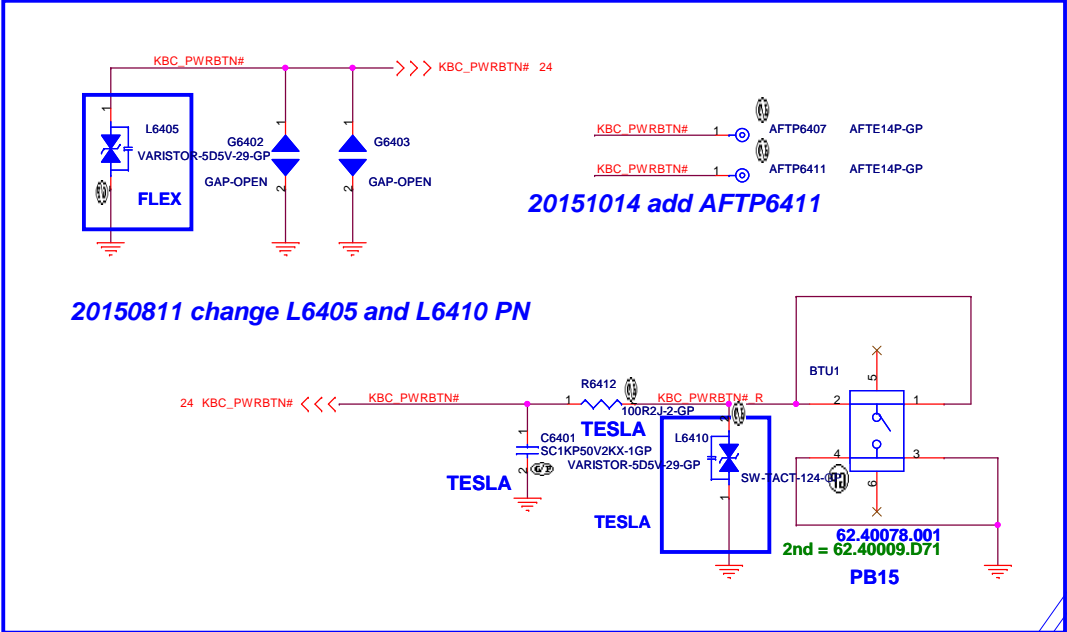
OSLO-SKLH

Rev SC

Date: Tuesday, August 25, 2015

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Power Button



POWER BTN LED

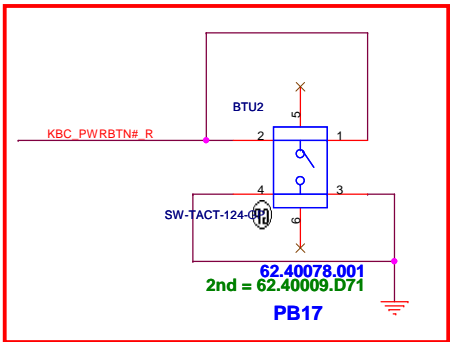
20150706 remove LED1 R6413 U6402

20150706 remove LED4

10/14 R6413 510R Change to 910R

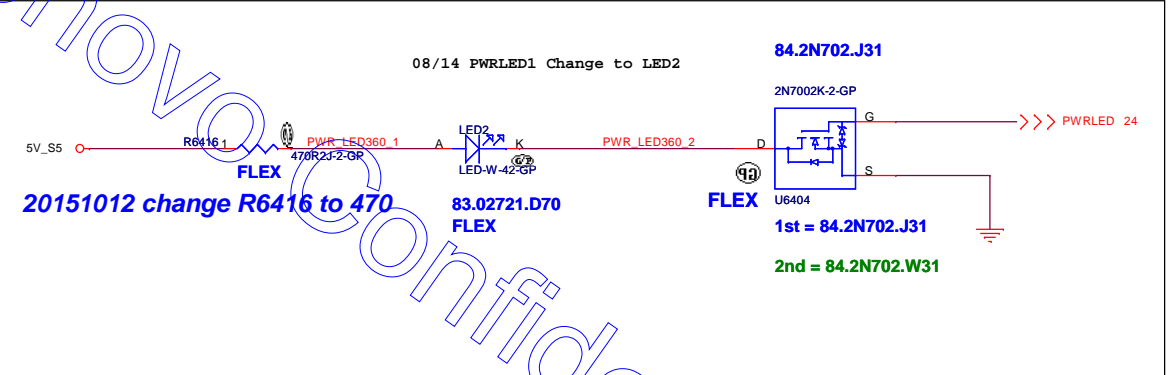
Symbol	Bin Code	Min.	Max.	Unit	Condition
Iv	P1	45	57	med	If=5mA
	P2	57	72		
	Q1	72	90		
	Q2	90	112		
Vf	28	2.60	2.70	V	If=5mA
	29	2.70	2.80		
	30	2.80	2.90		
	31	2.90	3.00		

Part No.	Chip		Lens Color
	Material	Emitted Color	
48-213/T3D-AP1Q2TY/3C	InGaN	Pure White	Yellow Diffused



20150526 reserve for 17

FLEX360 POWER BTN LED



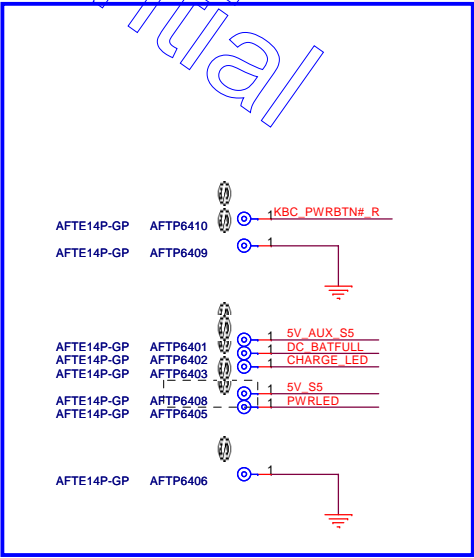
FLEX360 CHARGER LED

08/14 BATTLED1 Change to LED3

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward Voltage	Vf	S2S	1.7	2.3	V	If=5mA
		T3	2.7	3.3		

Chip Materials	Emitted Color
AlGaInP	Brilliant Orange
InGaN	Pure White

Test point



20150911 TP6404 change to AFTP6408

20150521 reserve KB2 for 17

[illegible]

Timing diagram for the TP module. The diagram shows the relationship between the AFTP module outputs and the TP module signals. The signals are:

- TP_SMB_DATA**: Data signal for the TP module.
- TP_SMB_CLK**: Clock signal for the TP module.
- TP_DATA**: Data signal for the TP module.
- TP_CLK**: Clock signal for the TP module.
- TouchPad**: Signal for the TouchPad module.

The diagram shows that the AFTP module outputs are connected to the TP module signals. The AFTP module outputs are:

- AFTP6539**: Connected to **TP_SMB_DATA**.
- AFTP6538**: Connected to **TP_SMB_CLK**.
- AFTP6536**: Connected to **TP_DATA**.
- AFTP6537**: Connected to **TP_CLK**.
- AFTP6533**: Connected to **TouchPad**.
- AFTP6532**: Connected to **TouchPad**.

Pin assignment diagram for the PS/2 connector. The diagram shows a 6-pin connector with pins numbered 1 to 6. The pin assignments are as follows:

PIN NO.	SIGNAL
1	VDD (3.3V)
2	PS2_CLK
3	PS2_DAT
4	GND
5	NC
6	NC

A red box highlights the connector area with a dimension H=1.3. A circular symbol with a crosshair is shown below the connector.

24 KB_BKLT_PWM >>> KB_BKLT_PWM

U6503

BK

2N7002K-2-GP

84.2N702.J31

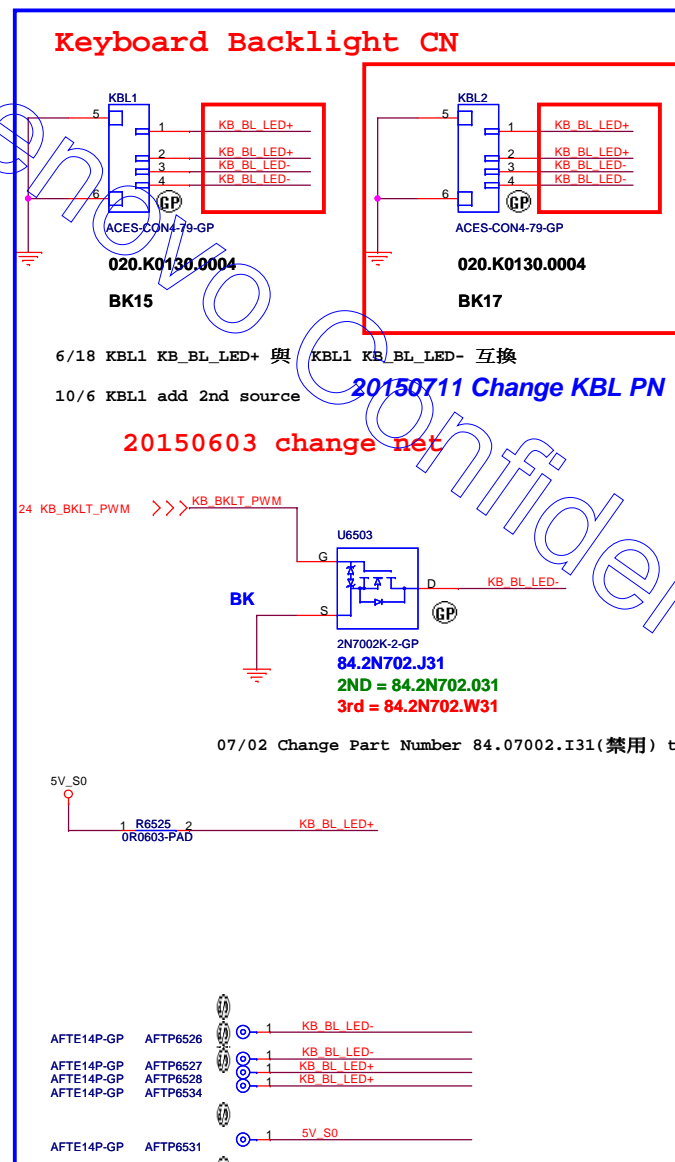
2ND = 84.2N702.031

3rd = 84.2N702.W31

KB BL LED

U6203

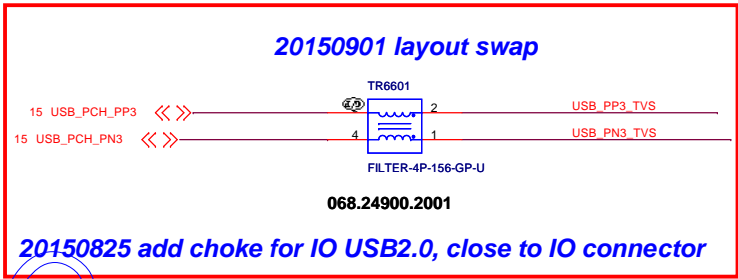
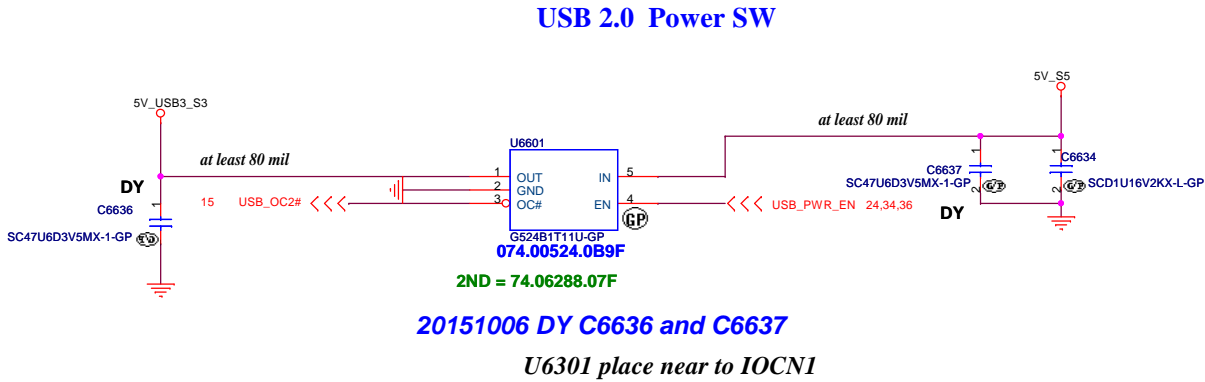
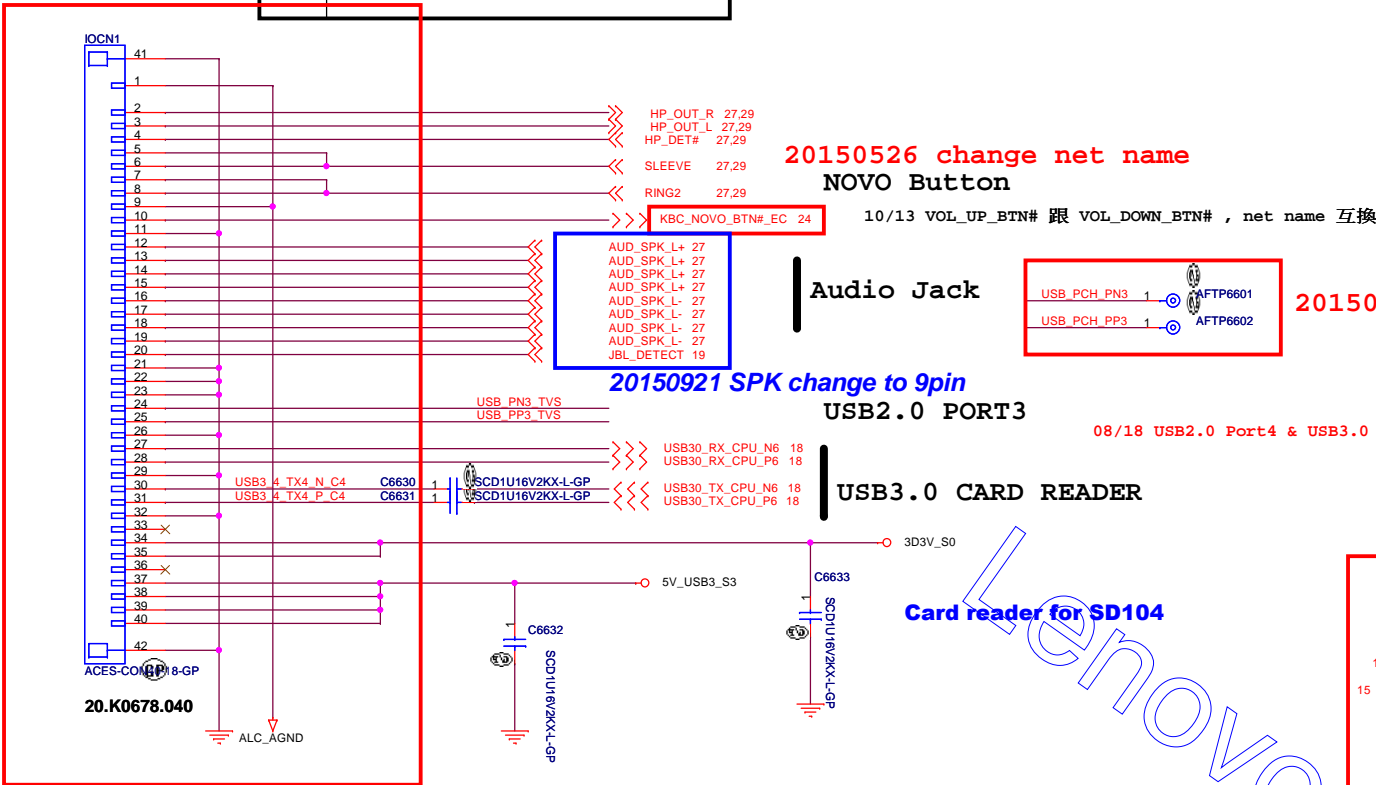
07/02 Change Part Number 84.07002.I31(禁用) to 84.2N702.J31



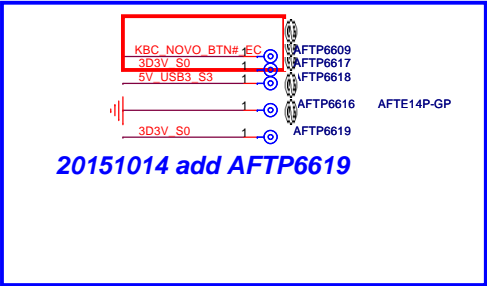
The image displays two wiring diagrams for the K0035.0030 component, labeled KB2 (left) and KB1 (right). Both diagrams show a vertical connector with pins 1 through 32. The left diagram (KB2) shows connections for KROW 1 through 7, KCOL 0 through 15, and LED/C pins 26 through 30. The right diagram (KB1) shows similar connections but includes additional components: R6511, R2J-3-GP, and 330R2J-3-GP. The diagrams are color-coded: blue for power/ground, red for signal, and green for LED/C pins. The component is identified as 020.K0035.0030 and the board is labeled KB17 (left) and KB15 (right).

IO BD Device

Item	Device
1	NOVO Button
2	Audio Jack
3	USB Card Reader
4	USB2.0 Port4

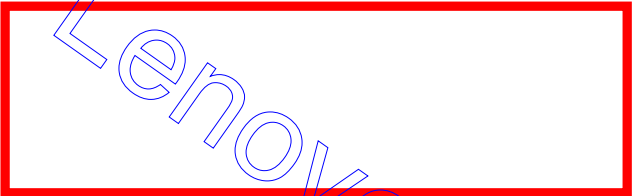


Test point




5					4					3					2					1				
D																								
C																								
B																								
A																								
5					4					3					2					1				

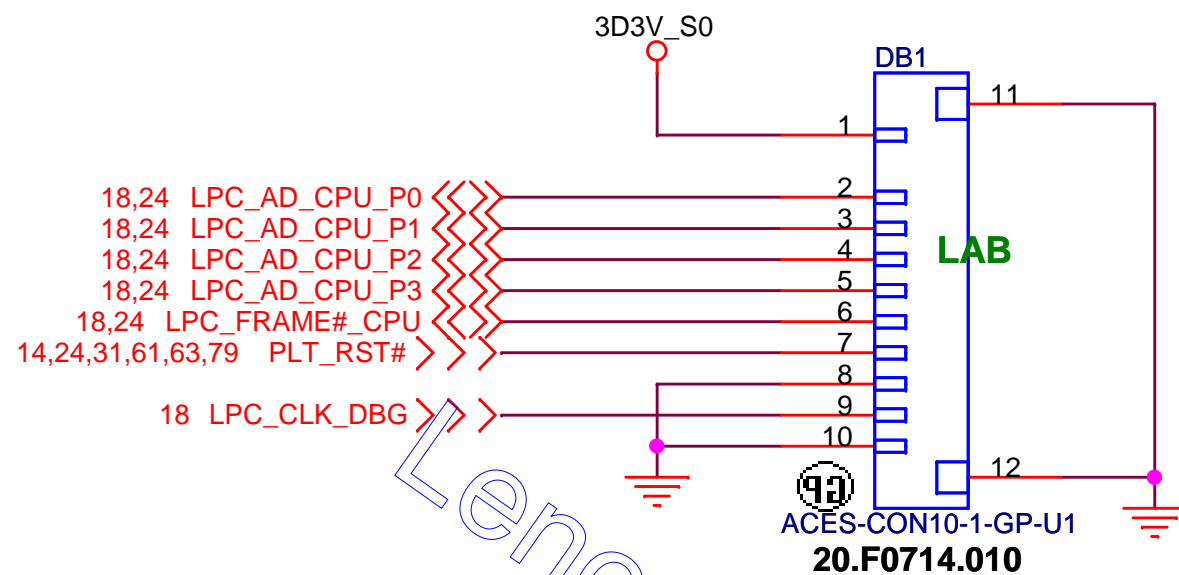
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20150603 remove

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Title			
<i>Hall Sensor</i>			
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Title

Debug connector

Size
A

Document Number

OSLO-SKLH

Rev

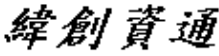
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Title G-SENSOR			
Size A3	Document Number OSLO-SKLH		Rev SC
Date: Saturday, July 11, 2015		Sheet 69 of	105

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Title

(Reserved)Free Fall Sensor

Size
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Document Number

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Rev

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Title			
Thunderbolt(2/5)			
Size	Document Number		Rev
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Date: Saturday, July 11, 2015			
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Title

(Reserved) Thunderbolt (4/5)

Size
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Document Number

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5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

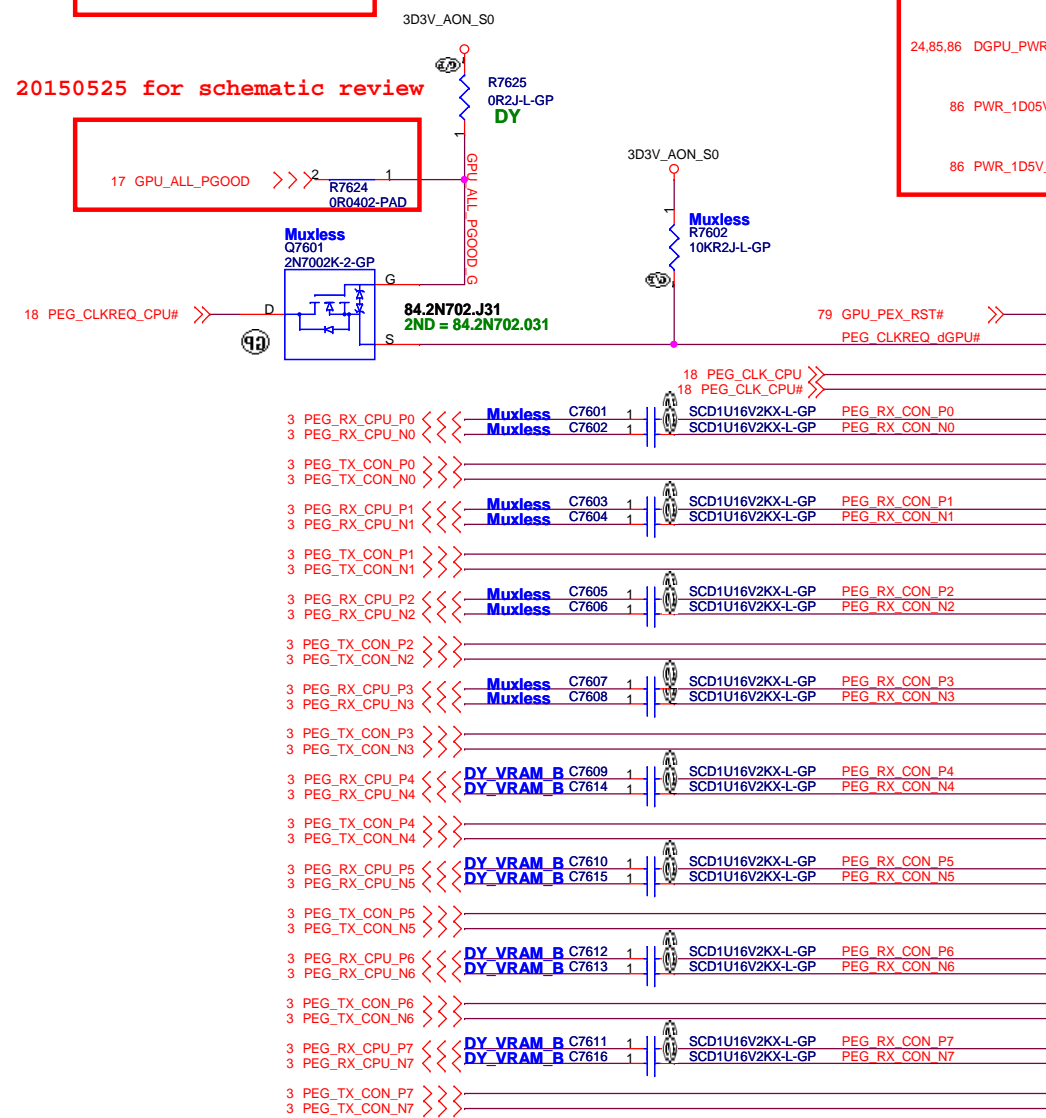
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Title (Reserved)Thunderbolt (5/5)			
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20150525 remove schematic

20150525 for schematic review



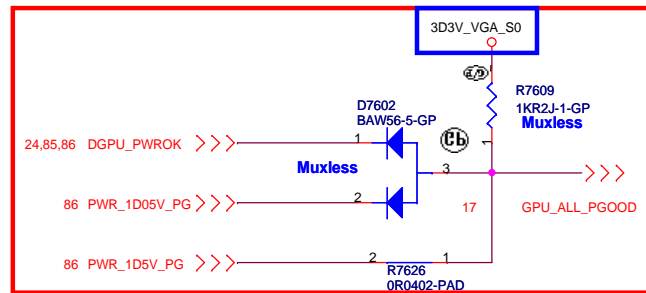
3.4.2 PCI Express Power Decoupling and Filtering

Table 3-16. PEX_IOVVD/Q Power Rail Combined

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB2B-64	1.0 μ F	X6S	0402	1
	4.7 μ F	X6S	0603	1
	10 μ F	X5R	0805	1
	22 μ F	X5R	0805	1
GB4B-128 GB3-256	1.0 μ F	X6S	0402	4
	4.7 μ F	X6S	0603	2
	10 μ F	X5R	0805	4
	22 μ F	X5R	0805	4

Table 3-18. PEX_SVDD_3V3 and PEX_PLL_HVDD Decoupling

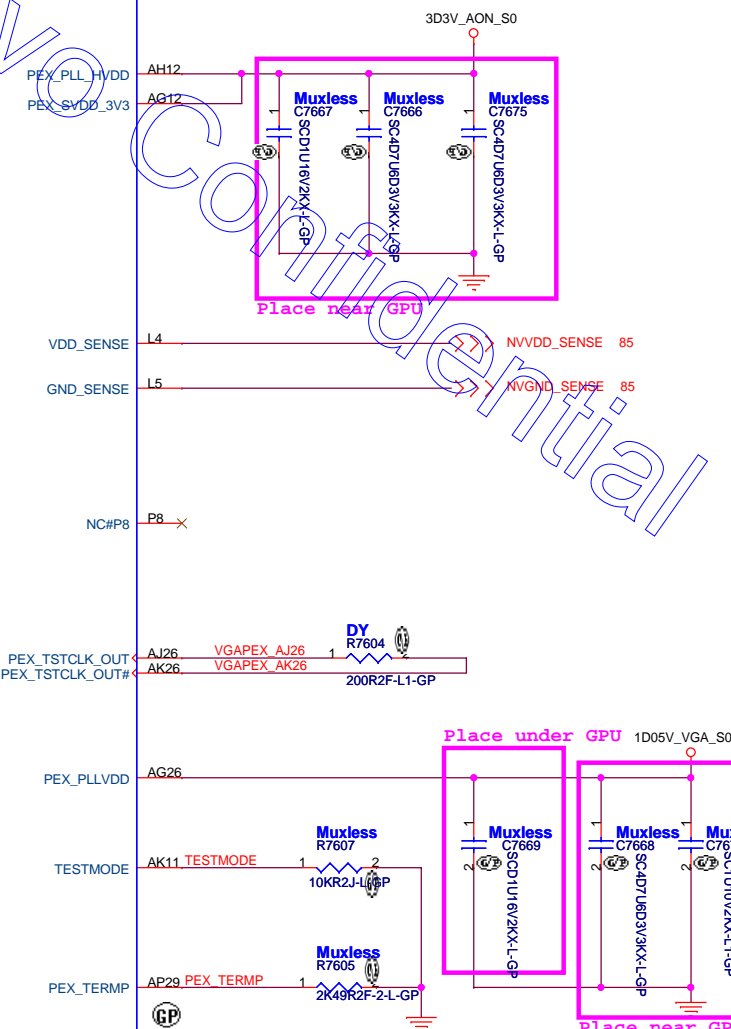
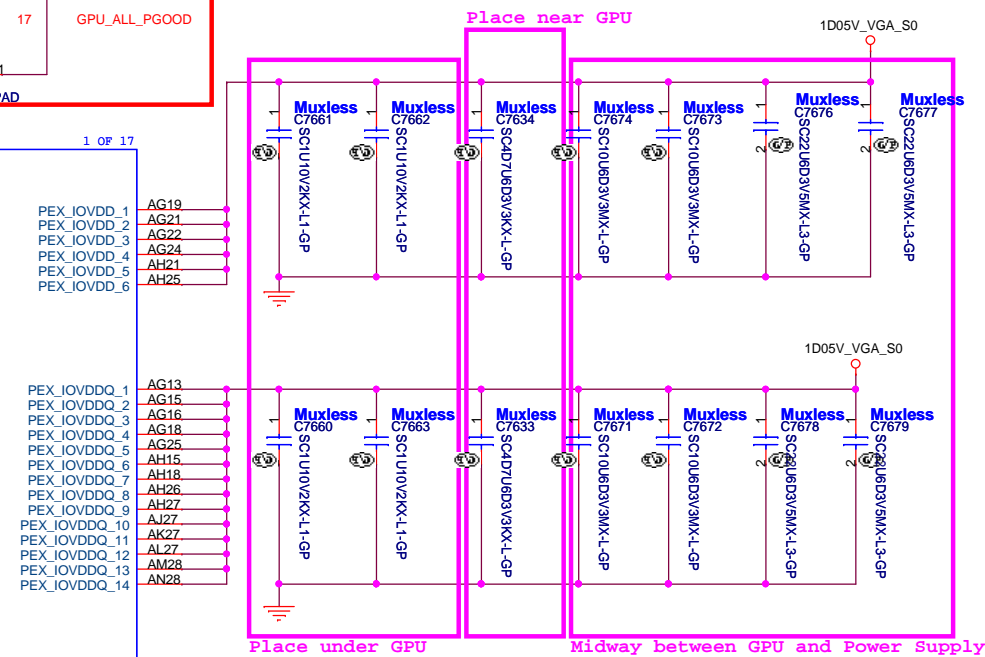
Capacitor Type	Footprint	Population	Location
0.1 μ F	X5R	0402	1
4.7 μ F	X5R	0603	2



20150617 NV modify power rail

20150527 add NV schematic

20150624 swap 1D5V PG and 1D05V PG



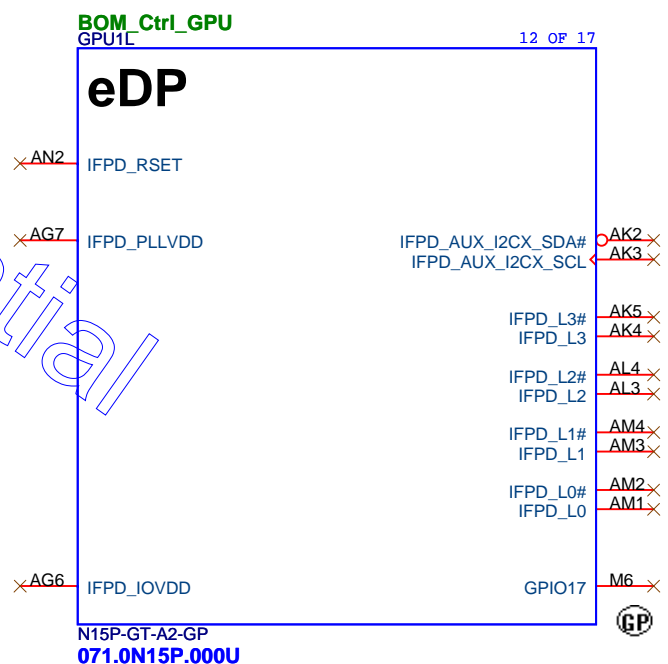
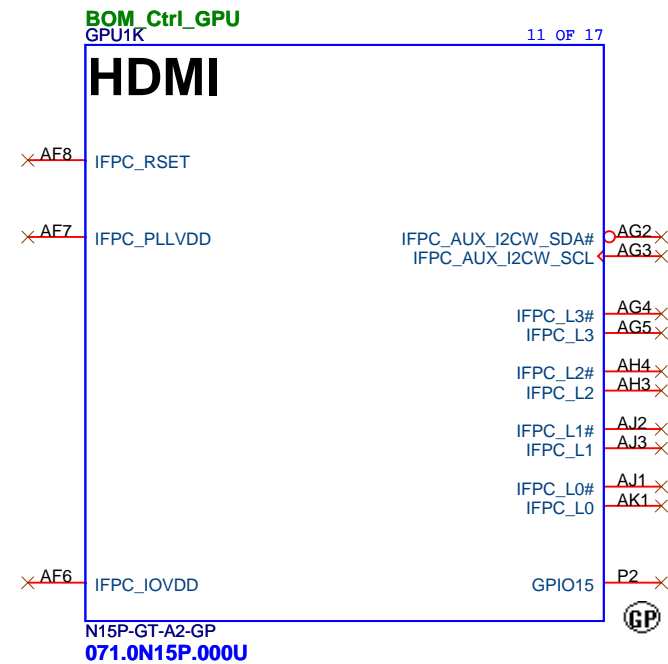
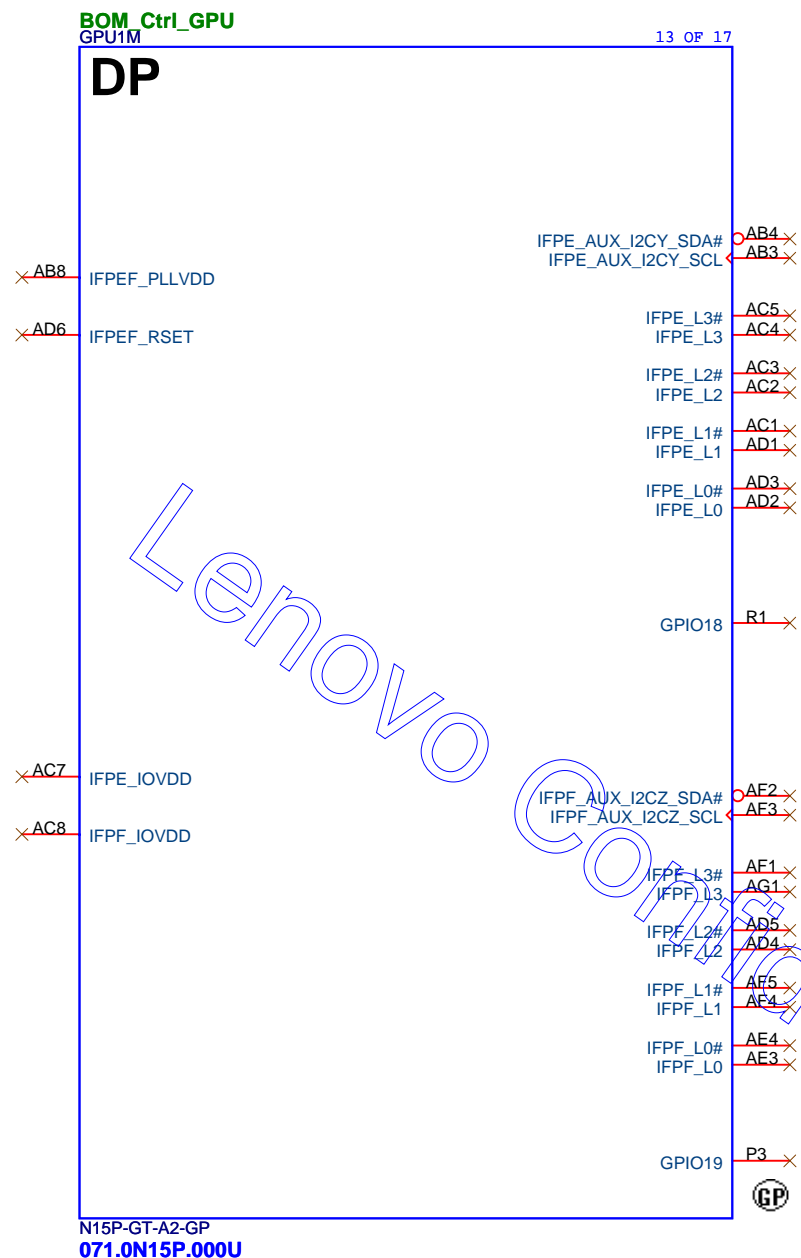
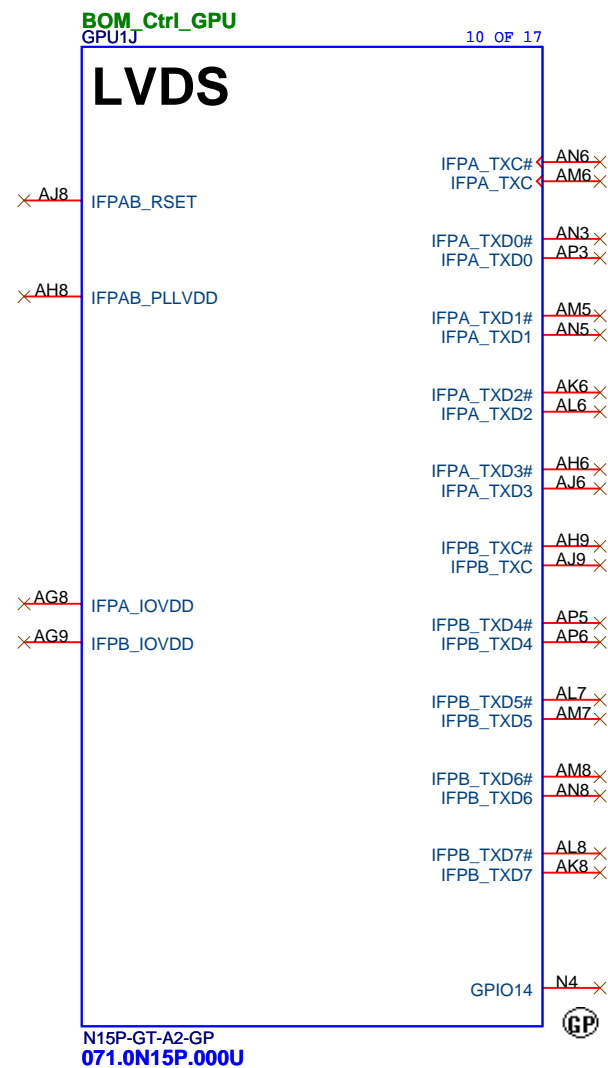
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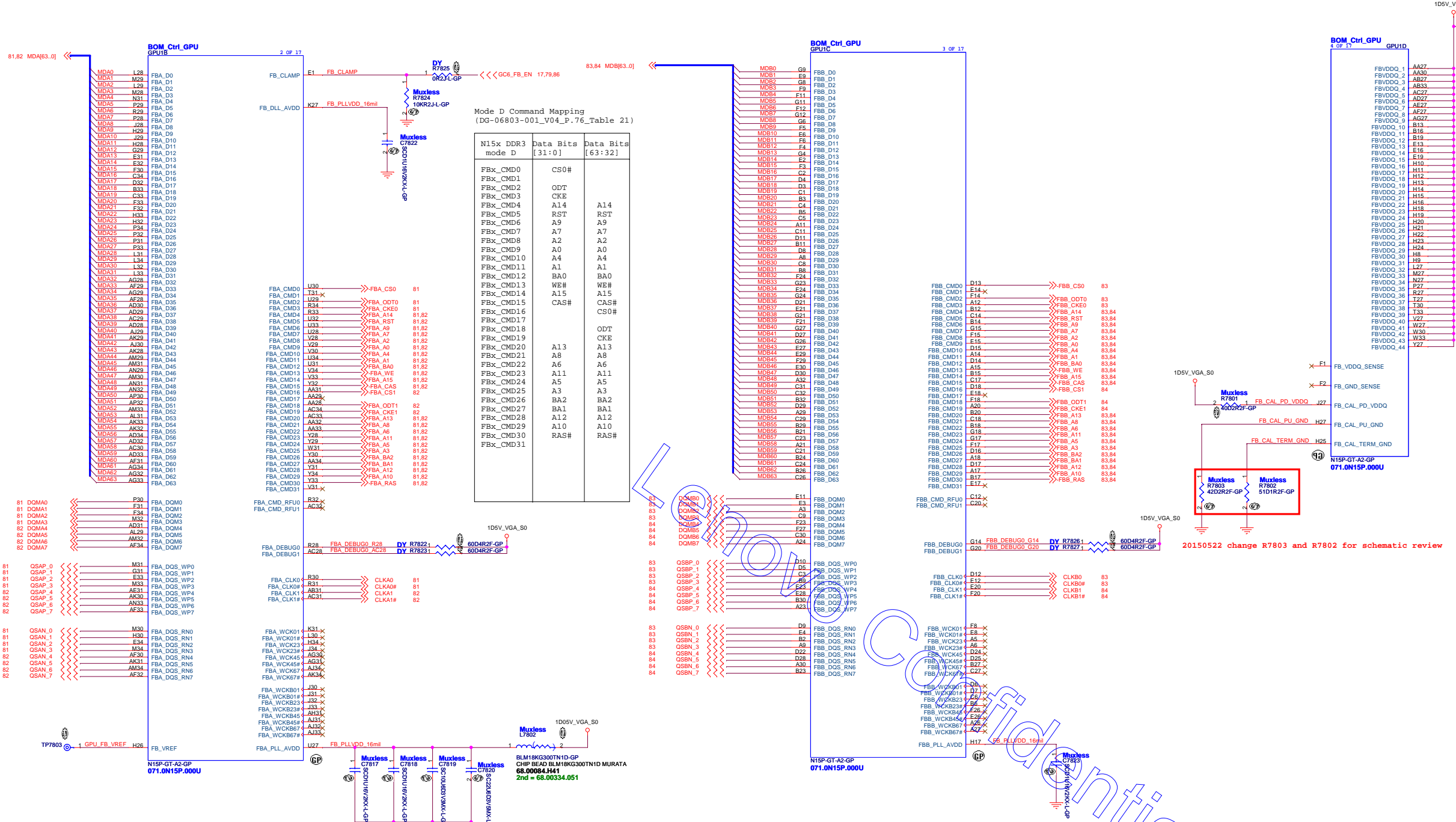
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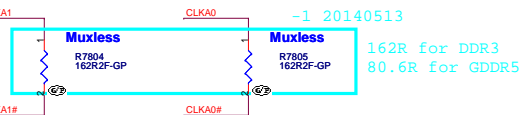


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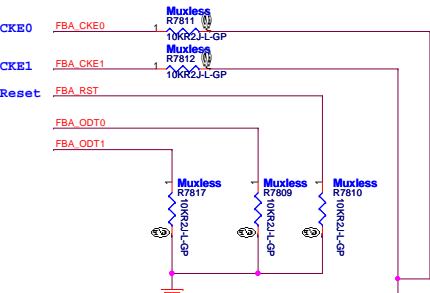
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Size A3	Document Number OSLO-SKLH	Rev SC	
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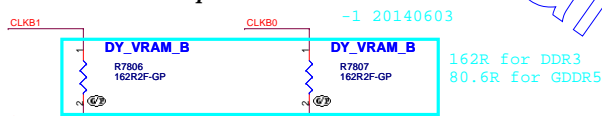
FBCLK Termination place on VRAM side



Group A



FBCLK Termination place on VRAM side



Group B

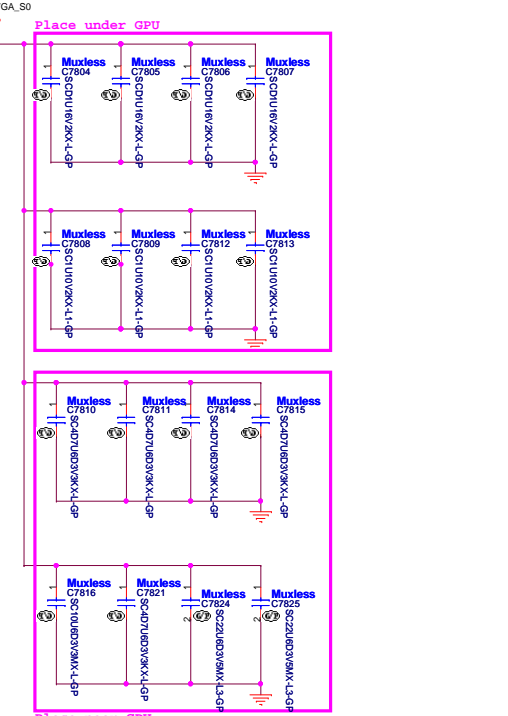
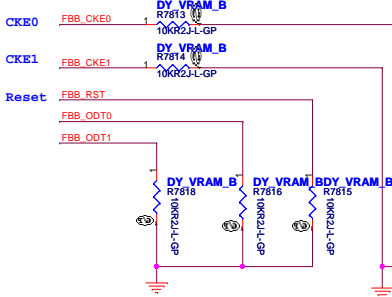


Table 3-10. GDDR5 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type	Footprint	Population	Location
GB28-64 GDDR5	0.1 μ F	X7R 0402	2	Under GPU
	1 μ F	X7R 0603	2	Under GPU
	4.7 μ F	X5R 0603	2	Under GPU
	10 μ F	X5R 0805	1	Under GPU
	22 μ F	X5R 0805	1	Near GPU
	47 μ F	X5R 0805	1	Near GPU
GB48-128 GDDR5	0.1 μ F	X7R 0402	4	Under GPU
	1 μ F	X7R 0603	4	Under GPU
	4.7 μ F	X5R 0603	4	Under GPU
	10 μ F	X5R 0805	2	Near GPU
	22 μ F	X5R 0805	2	Near GPU
	47 μ F	X5R 0805	2	Near GPU
GB3-256 GDDR5	0.1 μ F	X7R 0402	8	Under GPU
	1 μ F	X7R 0603	14	Under GPU
	4.7 μ F	X5R 0603	10	Under GPU
	10 μ F	X5R 0805	6	Near GPU
	22 μ F	X5R 0805	6	Near GPU
	47 μ F	X5R 0805	6	Near GPU

Notes:
1. At least two GND vias and two Power vias for each capacitor. All values in this table are preliminary; final values may change.
2. If a single partition 64-bit GPU in the GB48-128 package is used, populate only half of the recommended number of decoupling capacitors of GB48-128.

Table 3-14. FBX_PLL_AVDD and FB_DLL_AVDD Filtering

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB28-64	FBX_PLL_AVDD and FB_DLL_AVDD Combined	0.1 μ F	X7R 0402	2	Under GPU
		22 μ F	X5R 0805	1	Near GPU
		30 Ω (ESR<0.010 Ω)	0603	1	Near GPU
GB48-128	FBX_PLL_AVDD and FB_DLL_AVDD Combined	0.1 μ F	X7R 0402	3 (1 per ball)	Under GPU
		22 μ F	X5R 0805	1	Near GPU
		30 Ω (ESR<0.010 Ω)	0603	1	Near GPU
GB3-256	FBX_PLL_AVDD	0.1 μ F	X7R 0402	4 (1 per ball)	Under GPU
		22 μ F	X5R 0805	1	Near GPU
		30 Ω (ESR<0.010 Ω)	0603	1	Near GPU

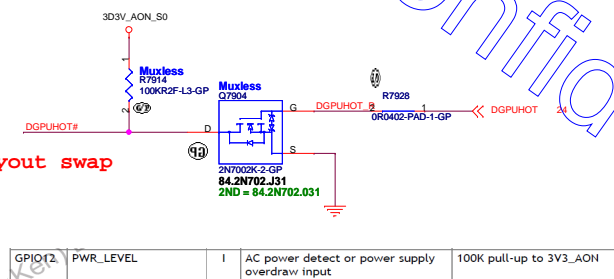
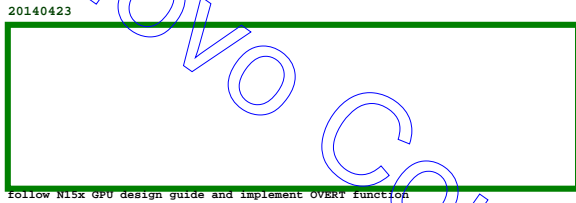
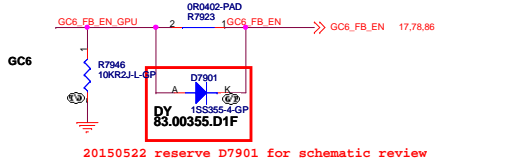
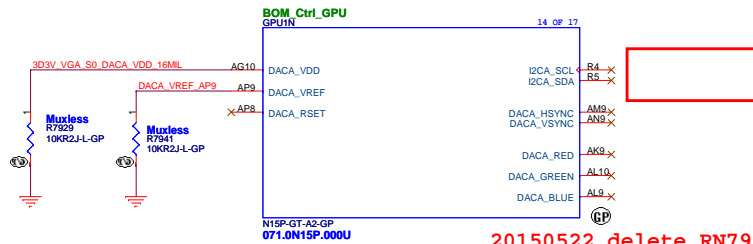
Note: Filtering for FBX_PLL_AVDD on GB3-256 is combined with PLL filtering in section 3.9.2.

Table 3-32. GB2B-64 and GB4B-128 PLLVDD Filtering

GPU Package	PLL Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 and GB4B-128	PLLVDD	0.1 μ F X7R	0402	1	Under GPU
		22 μ F X5R	0805	1	Hear GPU
		Bead Type	30 Ω (ESR=0.05)	0402	1
					Hear GPU

Table 3-33. SP_PLLVDD and VID_PLLVDD Power Rail Filtering Combined

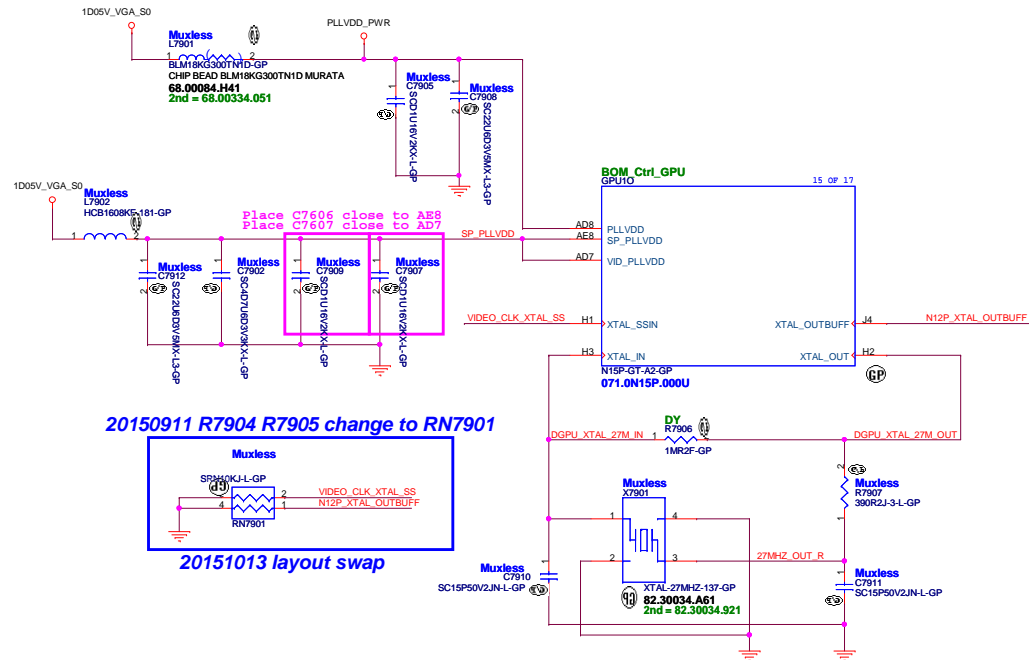
GPU Package	PLL Rails	Capacitor Type	Footprint	Population	Location
GB2B-64	SP_PLLVDD + VID_PLLVDD	0.1 μ F X7R	0402	1 per ball	Under GPU
GB4B-128		4.7 μ F X5R	0603	1	Hear GPU
GB3-256		22 μ F X5R	0805	1	Hear GPU
		Bead Type	180 Ω (ESR=0.2)	0603	1
					Hear GPU



GPIO[2]	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 3V3_AON
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20150525 add GPU reset for schematic review



DDR3

1.5V/1.5V

Single Rank

Hynix	H5TC4G63AFR-11C	A-die	0x0	1000	N/A	Production candidate
Micron	MT41J256M16HA-093G:E	E-die	0x1	1000	1322	Production candidate
Samsung	K4W4G1646D-BC1A	D-die	0x2	1000	N/A	Post-production candidate

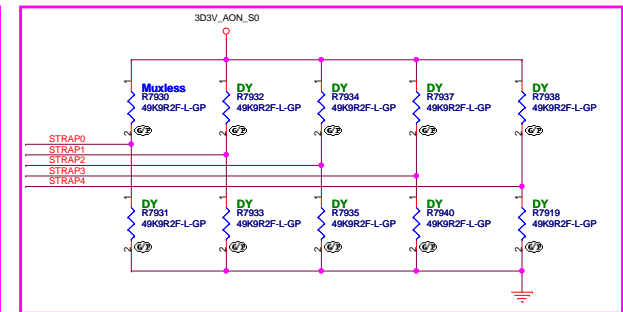
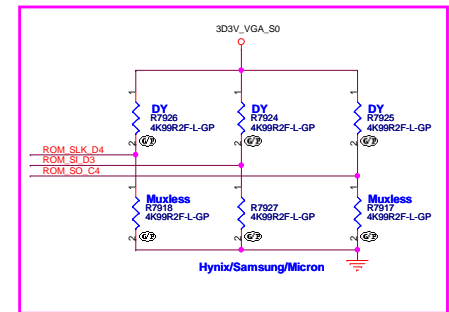
Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000 Hynix
10.0 k	1001	0001
15.0 k	1010	0010 Samsung
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

4.99Kohm 64.49915.6DL
10Kohm 64.10025.10L
15Kohm 64.15025.6DL
20Kohm 64.20025.6DL
24.9Kohm 64.24925.6DL
30.1Kohm 64.30125.6DL
34.8Kohm 64.34825.6DL
45Kohm 64.45325.6DL

Table 15-3. GB2B-64 and GB4B-128 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND and stuff 50k pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND for forward compatibility.			
STRAP2				
STRAP3				
STRAP4				



Hynix	H5TC4G63AFR-11C	A-die	0x0	1000
Micron	MT41J256M16HA-093G:E	E-die	0x1	1000
Samsung	K4W4G1646D-BC1A	D-die	0x2	1000

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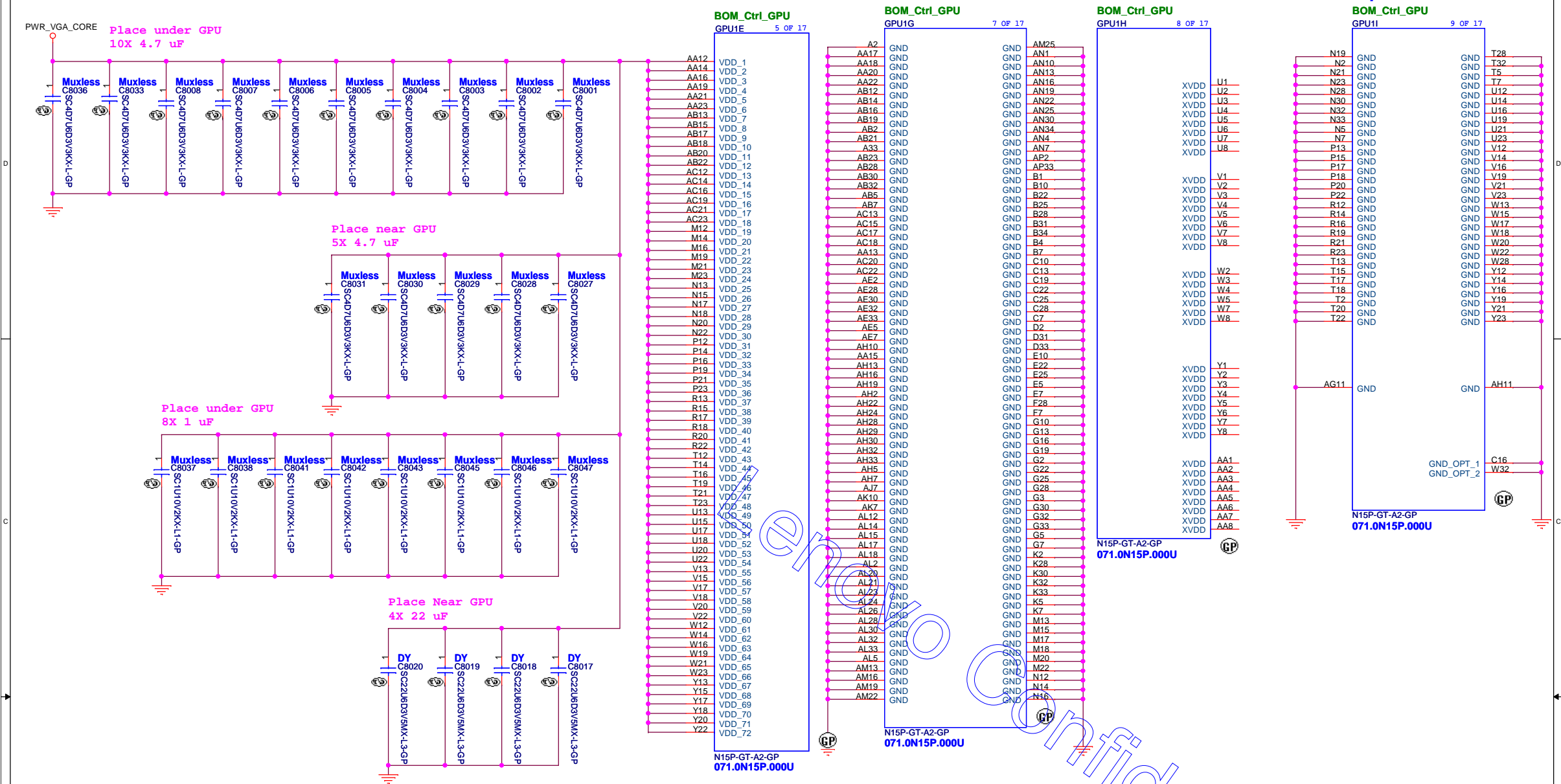


Table 3-6. NVVDD Decoupling Footprint and Population

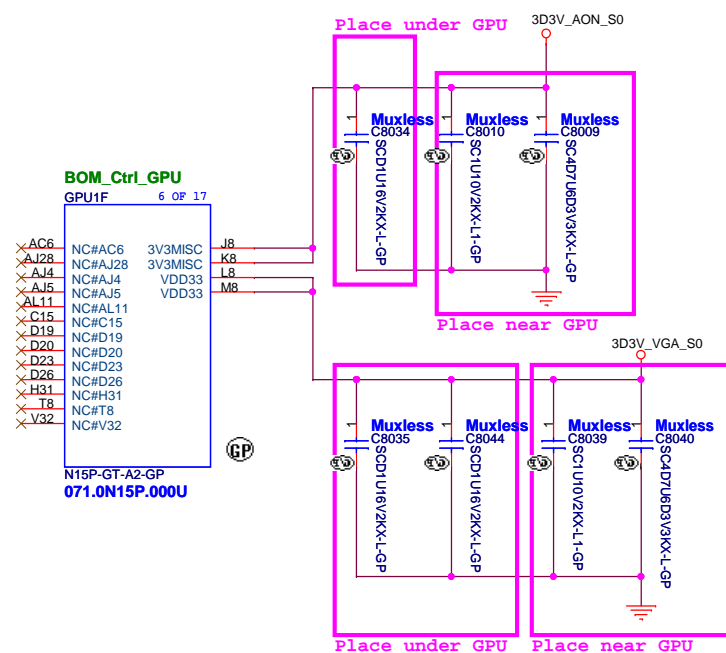
GPU Package Type	Capacitor Type	Footprint	Population	Location	Comments
GB2B-64	4.7 uF X65	0603	10	Under GPU	
	1 uF X65	0402	4	Under GPU	
	47 uF X5R	0805	1	Hear GPU	
	22 uF X5R	0805	1	Hear GPU	
	4.7 uF X5R	0805	5	Hear GPU	
GB4B-128	330 uF POS	7343	1	Hear GPU	ESR ≤ 6 mΩ
	4.7 uF X65	0603	15	Under GPU	
	1 uF X65	0402	8	Under GPU	
	22 uF X5R	0805	14	Hear GPU	See Note 2
	4.7 uF X5R	0805	7	Hear GPU	
GB3-256	330 uF POS	7343	2	Hear GPU	ESR ≤ 6 mΩ
	0.1 uF X7R	0402	20	Under GPU	
	4.7 uF X65	0603	40	Under GPU	
	10 uF X5R	0805	4	Hear GPU	
	22 uF X5R	0805	11	Hear GPU	
	400 uF X5R	1206	4	Hear GPU	
	330 uF POS	7343	4	Hear GPU	ESR ≤ 6 mΩ

Notes:
1. Generally the decoupling capacitor footprint requirement will remain the same but the population may get updated or may differ per GPU SKU. Always refer to the latest PUIH for any NVVDD decoupling requirement update for specific GPU SKUs.
2. Combine / co-layout two 0805 footprints into each of the POSCAP footprint. So a total of four 0805 footprints should be placed inside the two POSCAP foot prints, allocating fourteen 0805 footprints total.

Table 3-27. 3.3V Power Rail Decoupling

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1 uF X65	0402	2	Under GPU
		1 uF X5R	0603	1	Hear GPU
		4.7 uF X5R	0603	1	Hear GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1 uF X65	0402	1	Under GPU
		1 uF X5R	0603	1	Hear GPU
		4.7 uF X5R	0603	1	Hear GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.



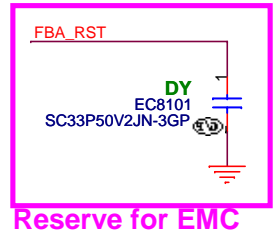
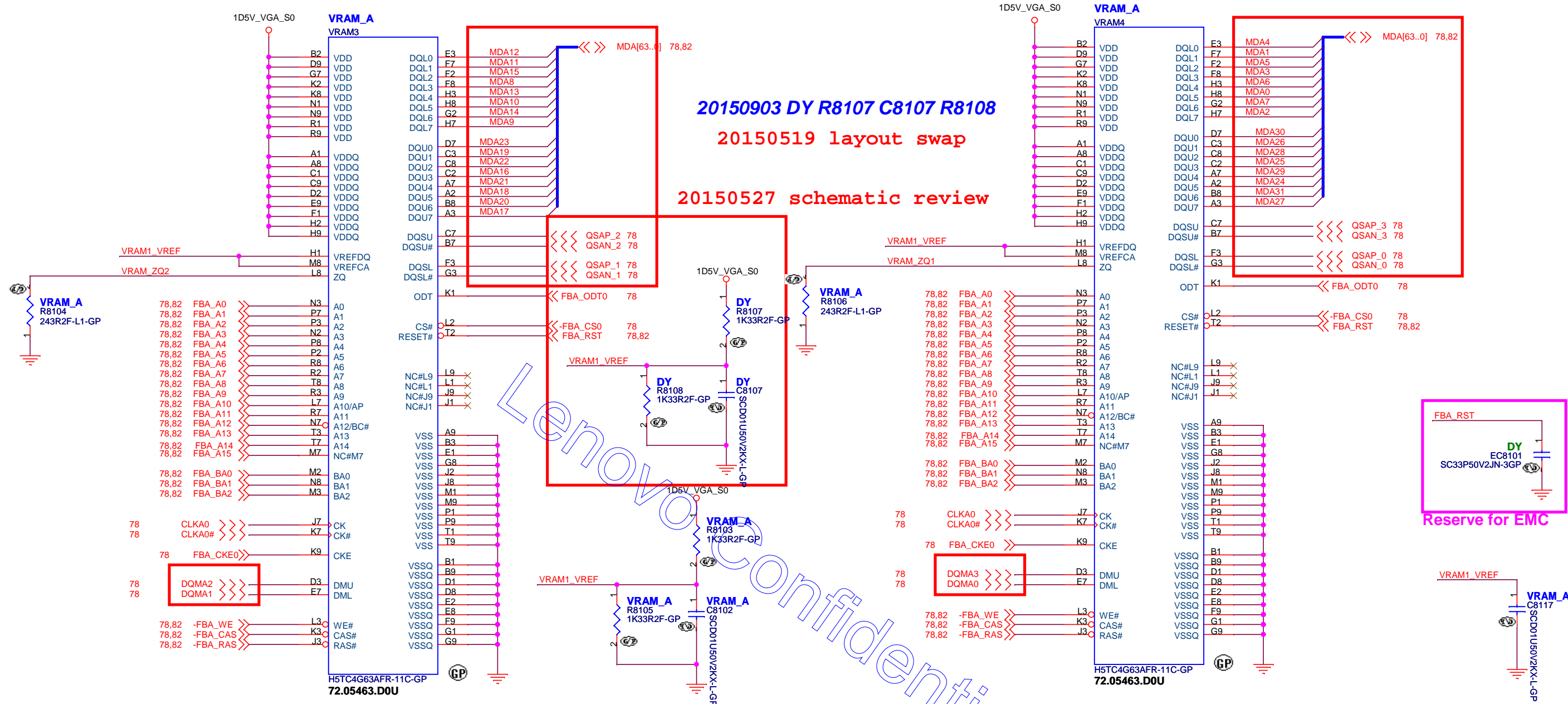
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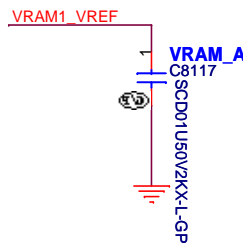
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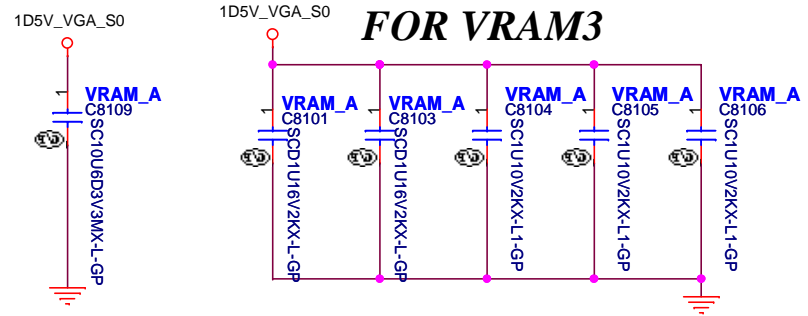
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Reserve for EMC



FOR VRAM3



FOR VRAM4

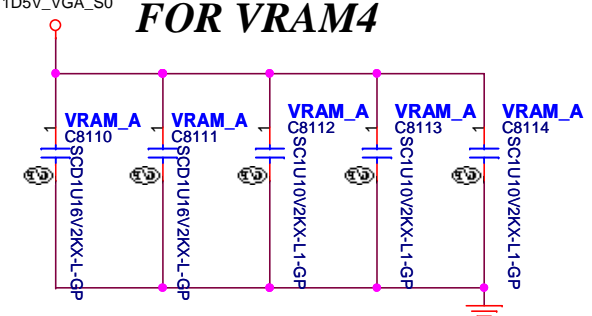
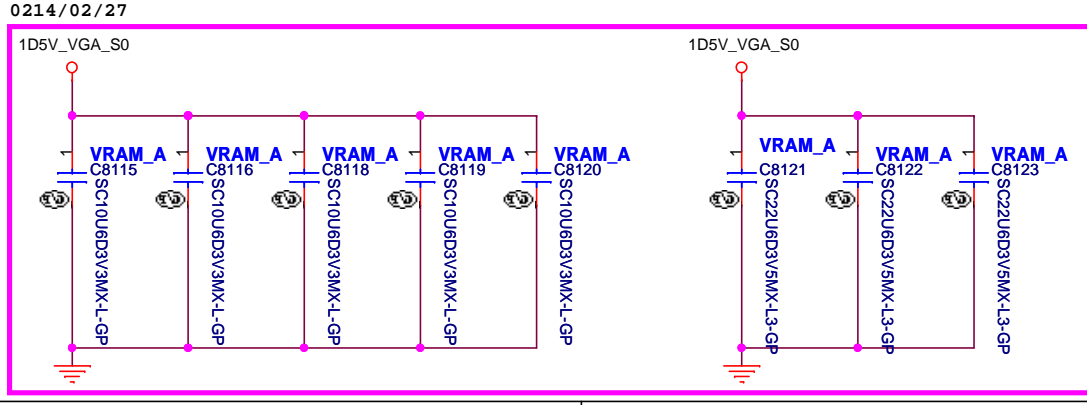


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDD/Q Combined					
0.1 μF	X7R	0402	2		Under DRAM
1.0 μF	X7R	0603	4		Under DRAM
10 μF	X5R	0805	0		Close to DRAM
FBVDD/Q Separato					
0.1 μF	X7R	0402	4	2	Under DRAM
1.0 μF	X7R	0603	3	1	Under DRAM
10 μF	X5R	0805	0	0	Close to DRAM
Note: *Location is close to DRAM for clamshell mode.					

Note: *Location is close to DRAM for clamshell mode.



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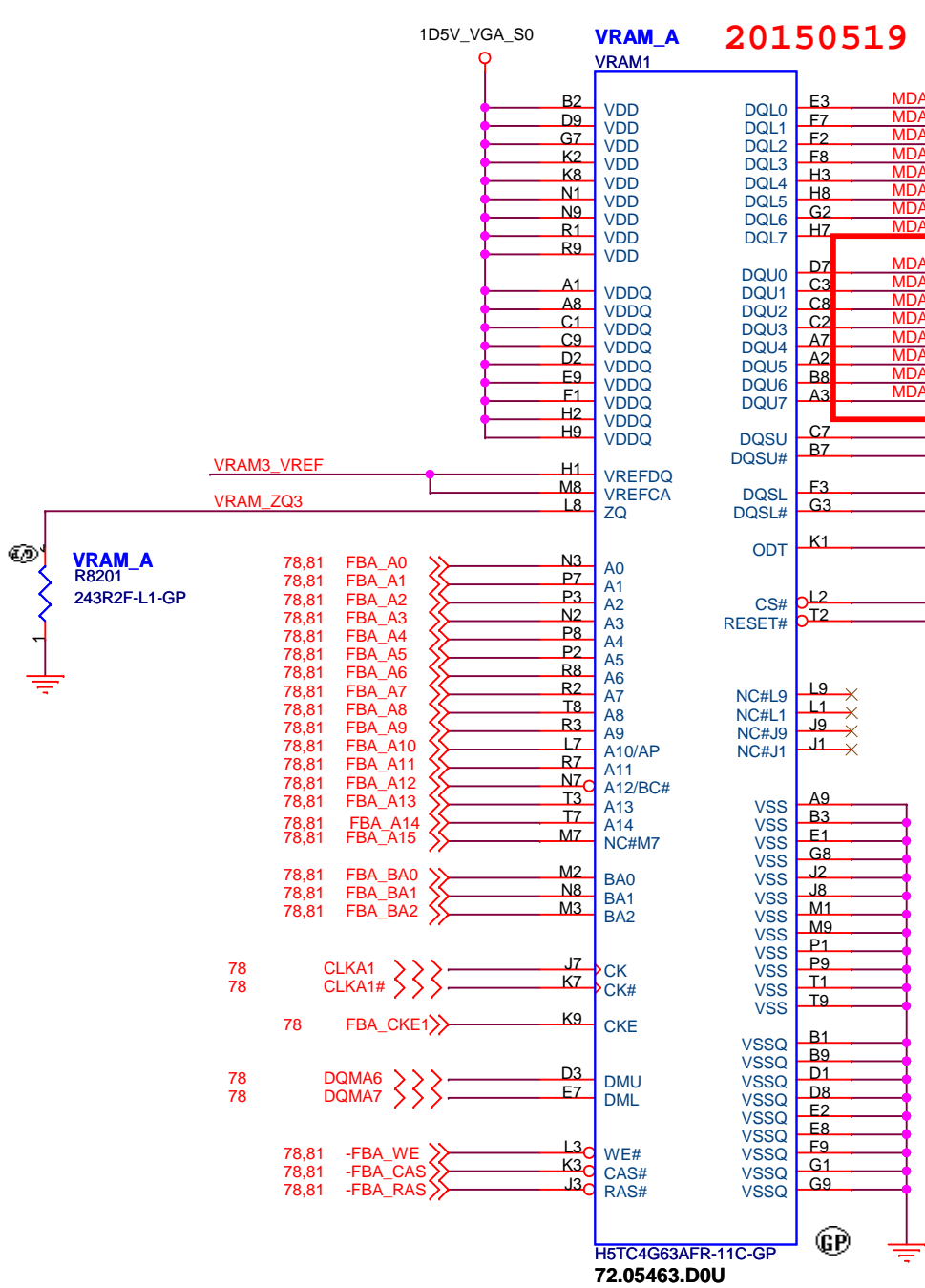
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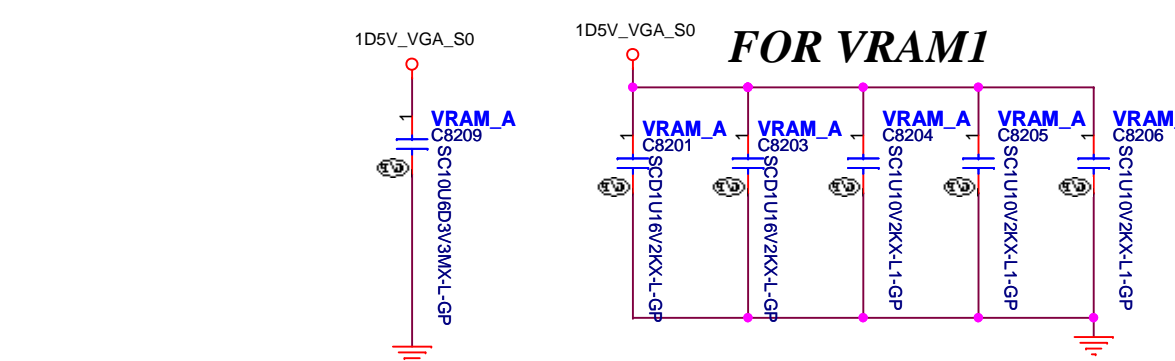
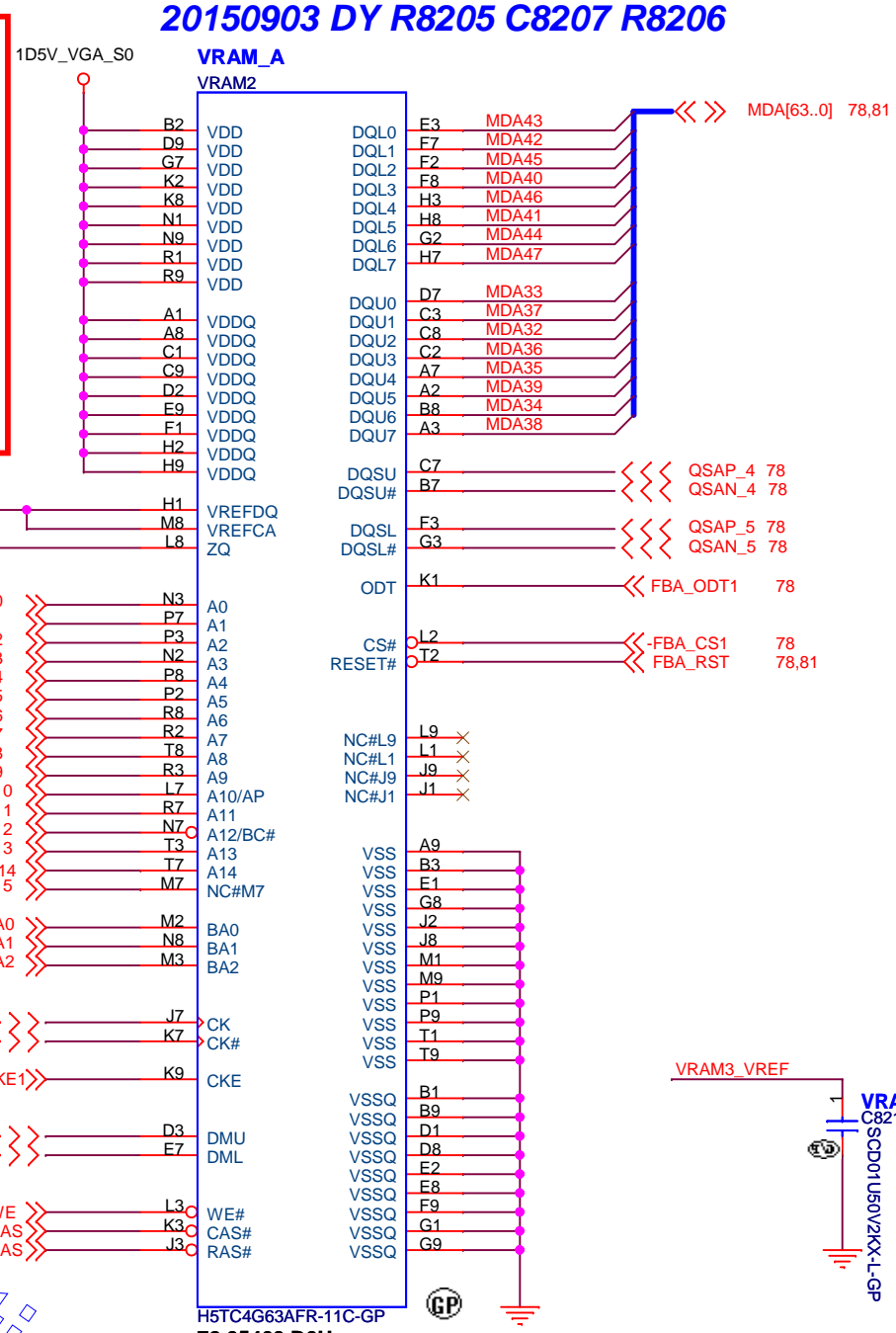
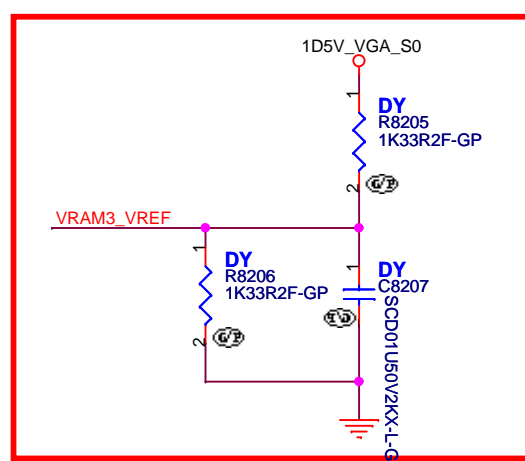
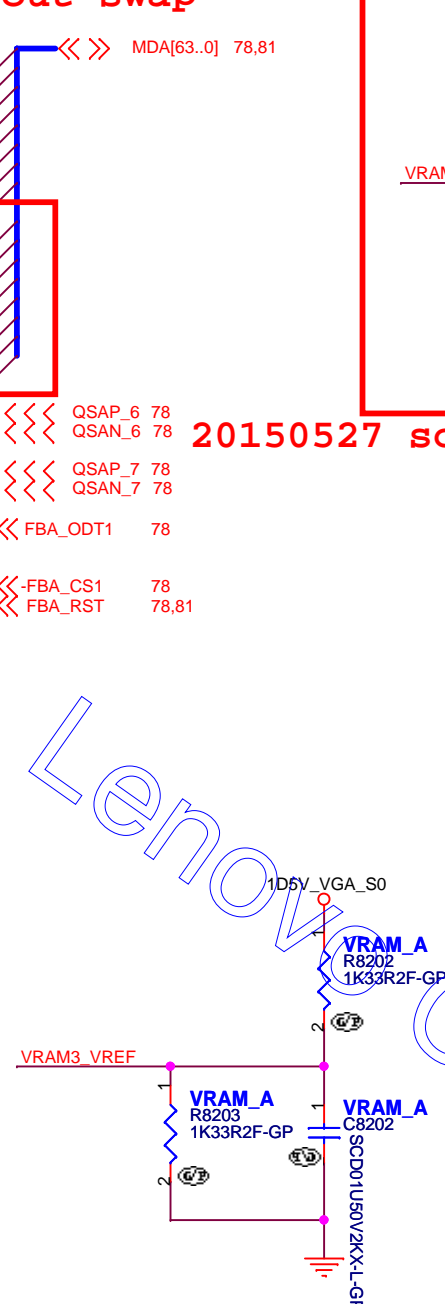
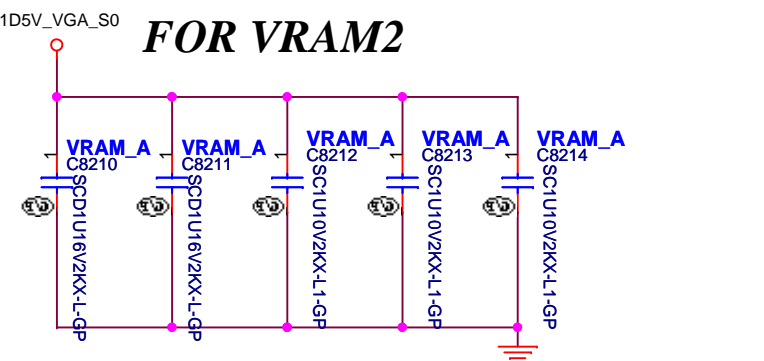


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type		Population		Location
		FBVDDQ	FBVDD	
FBVDD/Q Combined				
0.1 μ F	X7R	0402	2	Under DRAM
1.0 μ F	X7R	0603	4	Under DRAM
10 μ F	X5R	0805	0	Close to DRAM
FBVDD/Q Separate				
0.1 μ F	X7R	0402	4	Under DRAM
1.0 μ F	X7R	0603	3	Under DRAM
10 μ F	X5R	0805	0	Close to DRAM

Note: *Location is close to DRAM for clamshell mode.



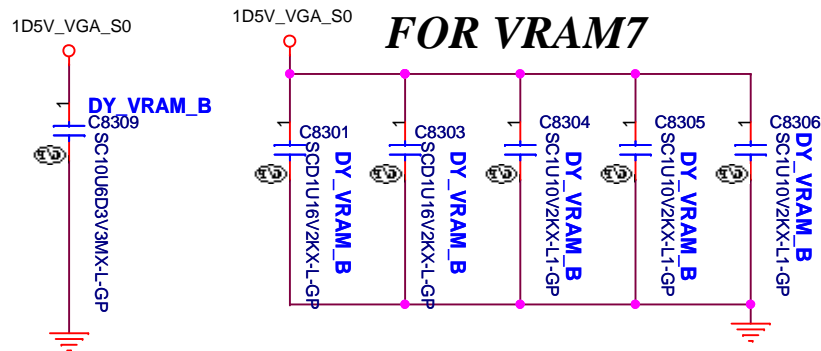
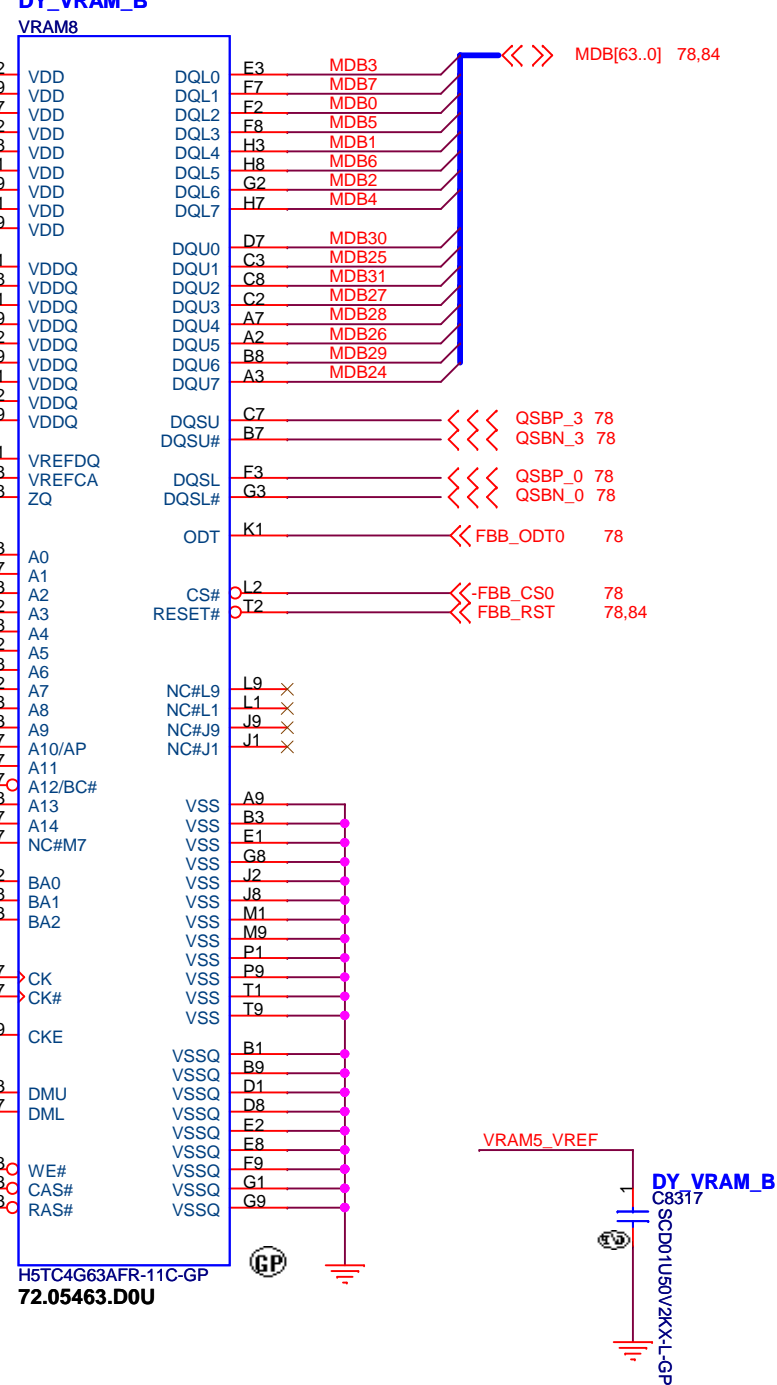
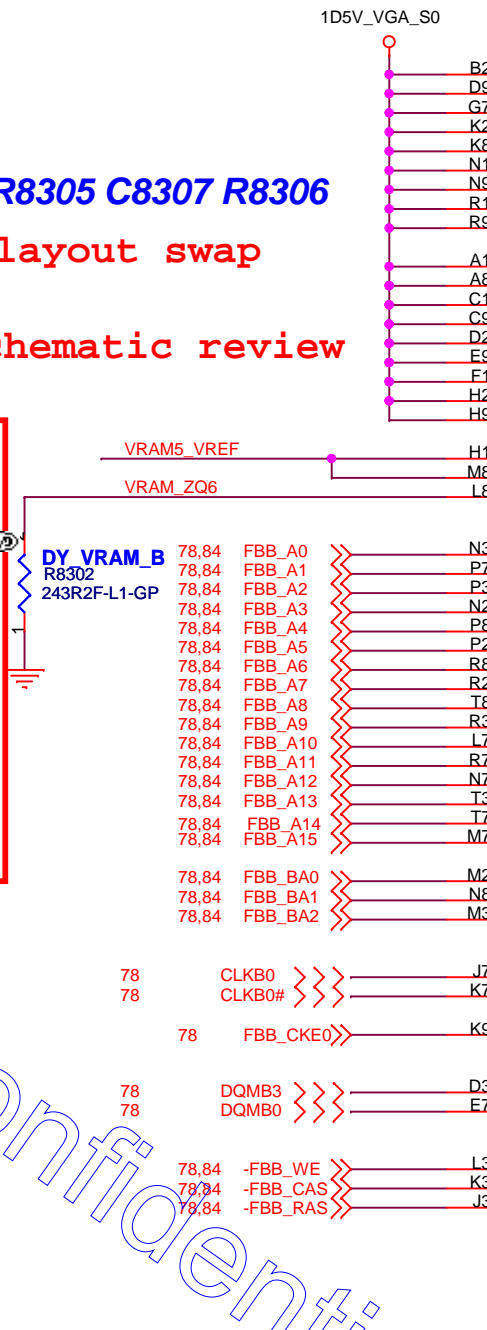
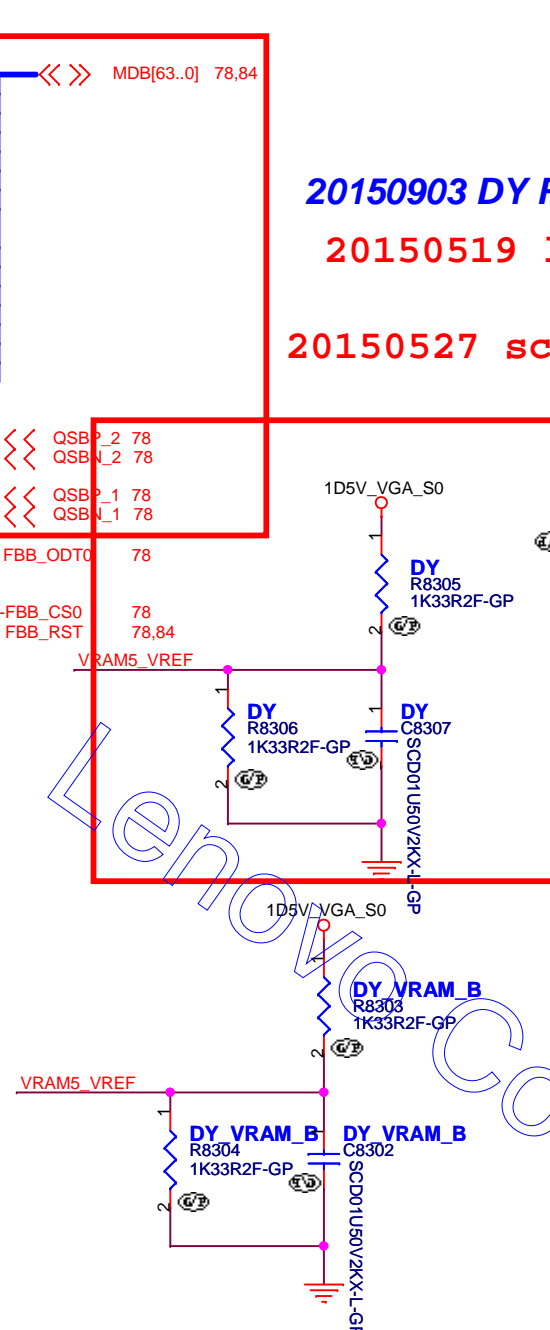
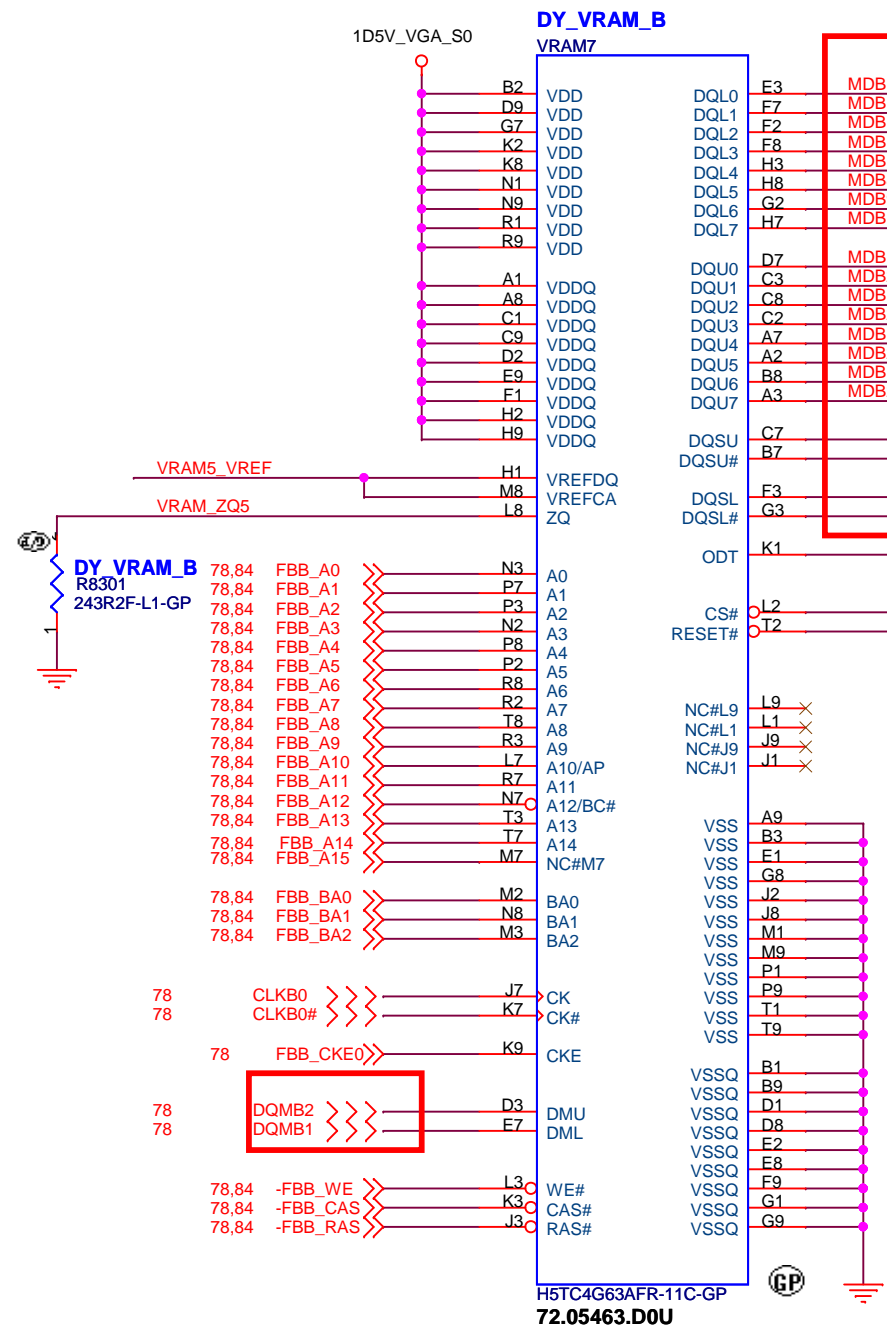
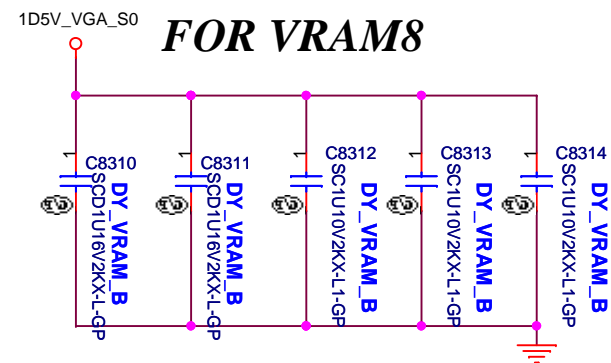


Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type			Population		Location
			FBVDDQ	FBVDD	
FBVDD/Q Combined					
0.1 μ F	X7R	0402	2		Under DRAM
1.0 μ F	X7R	0603	4		Under DRAM
10 μ F	X5R	0805	0		Close to DRAM
FBVDD/Q Separate					
0.1 μ F	X7R	0402	4	2	Under DRAM
1.0 μ F	X7R	0603	3	1	Under DRAM
10 μ F	X5R	0805	0	0	Close to DRAM
Note: *Location is close to DRAM, for clamshell mode.					

Note: *Location is close to DRAM for clamshell mode.



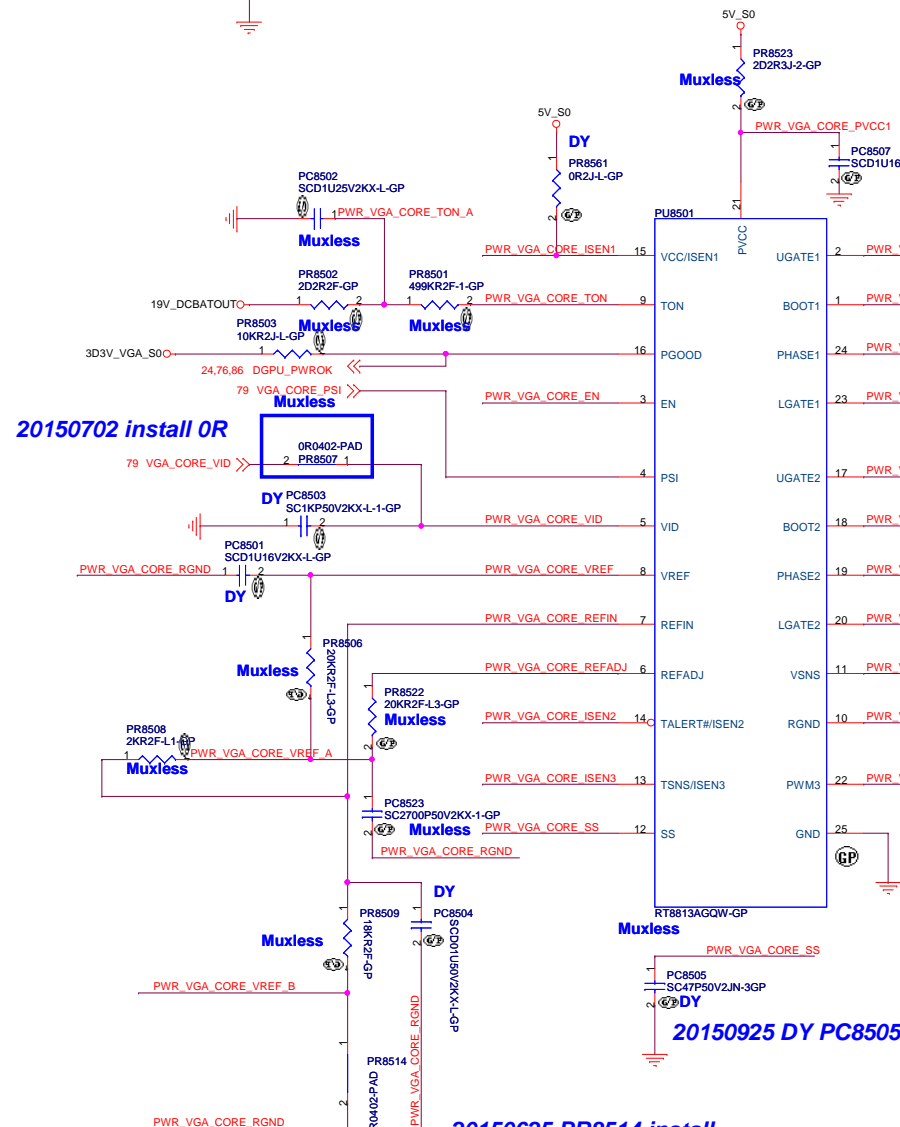
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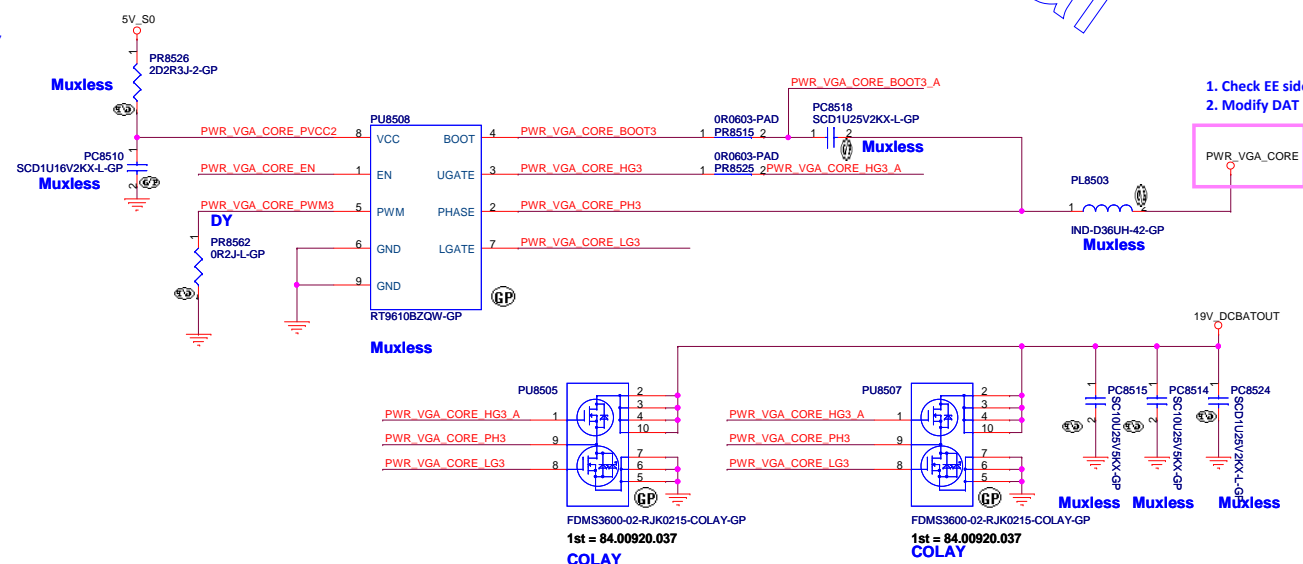
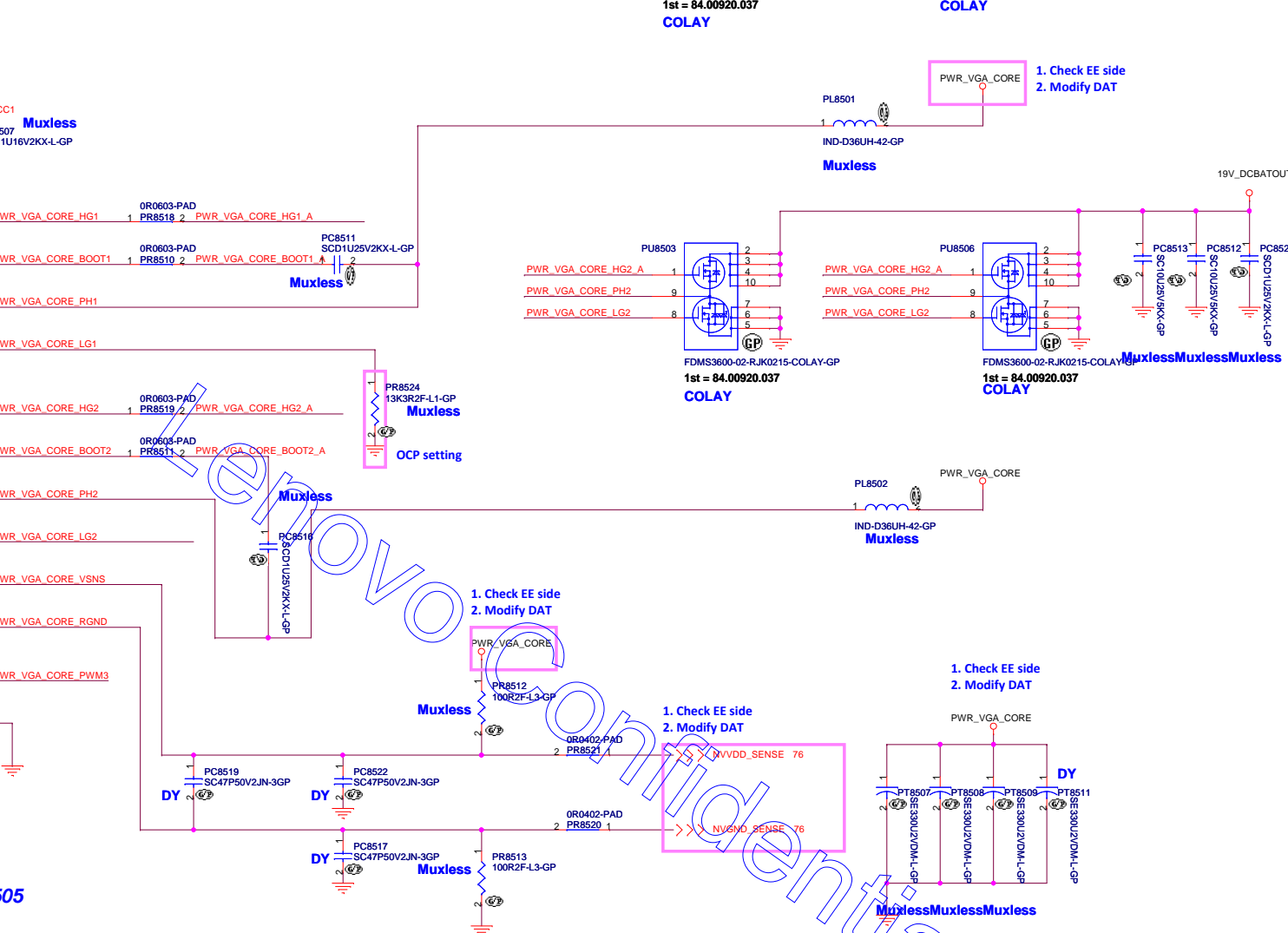
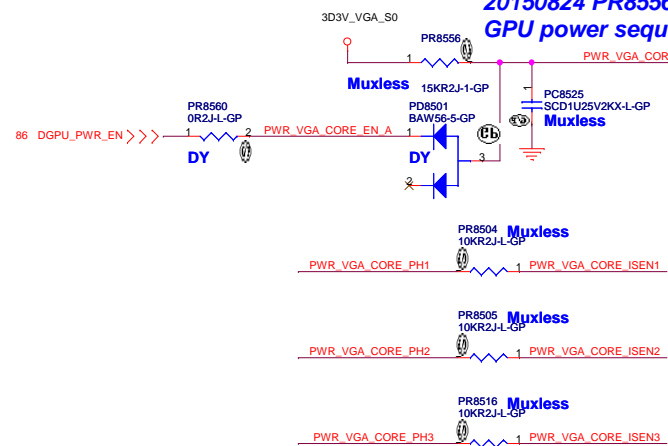
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PR8206	7.5k ohm	30k ohm	20k ohm
PR8208	0 ohm	3k ohm	2k ohm
PR8209	6.2k ohm	24k ohm	18k ohm
PR8214	1.74k ohm	3k ohm	0 ohm
PC8223	5.6nF	1.8nF	2.7nF



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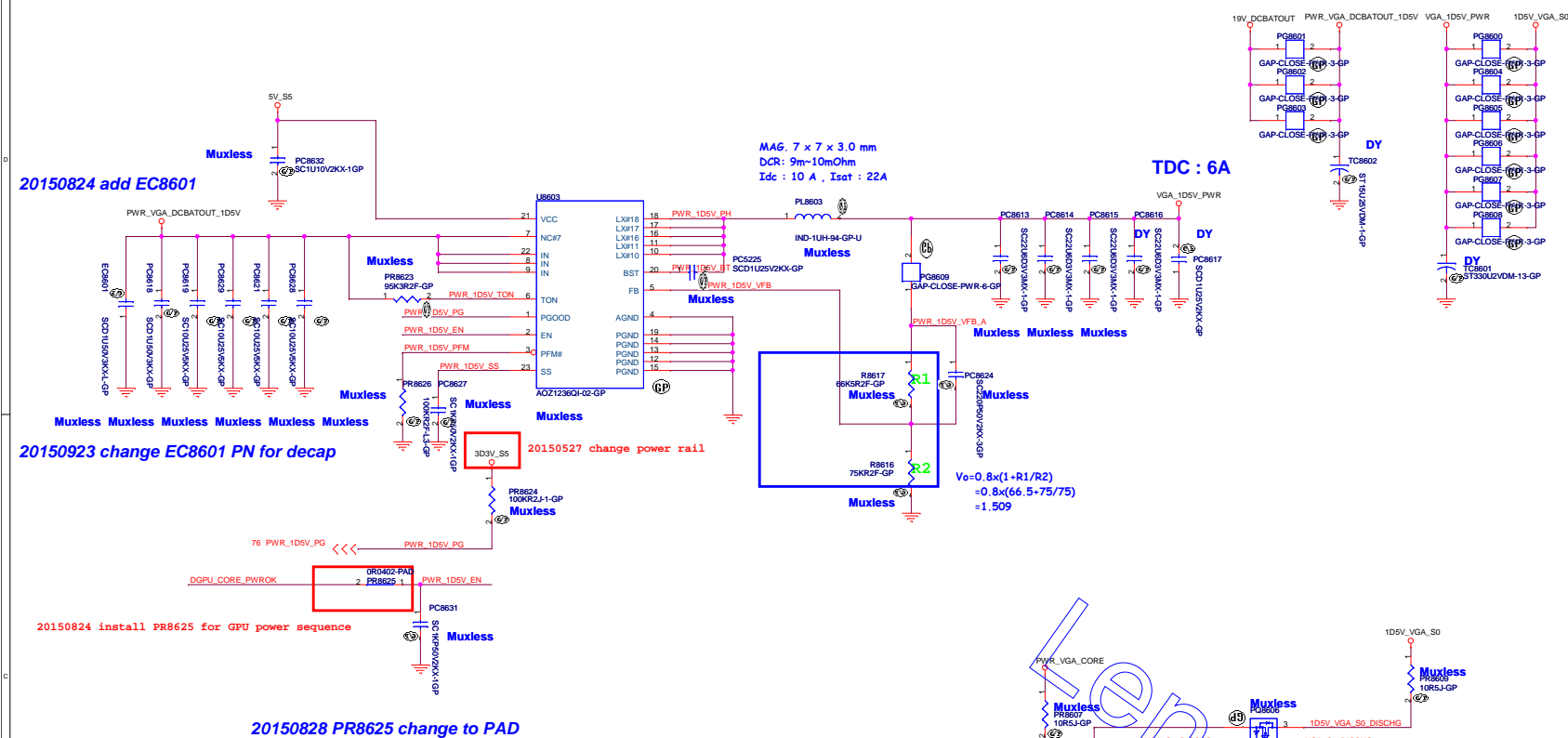
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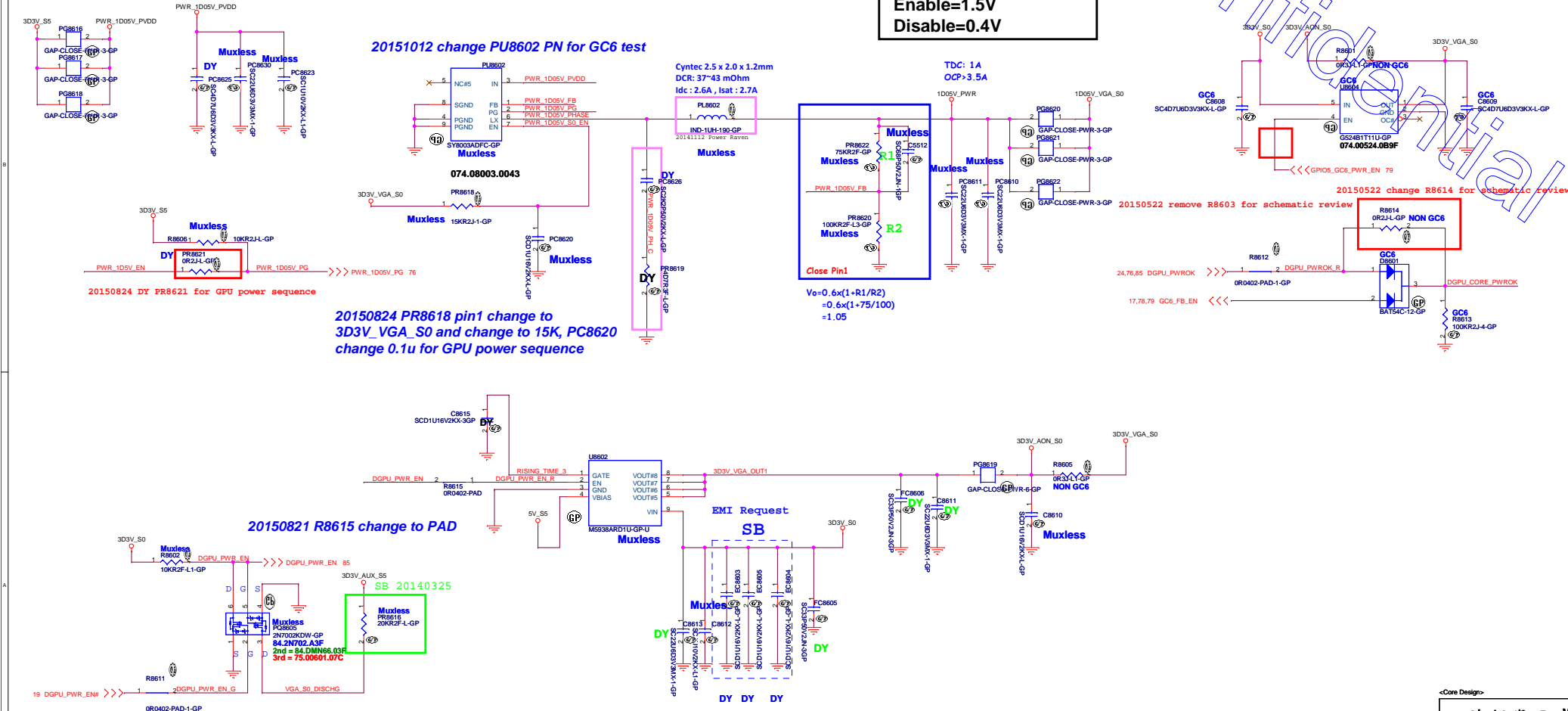
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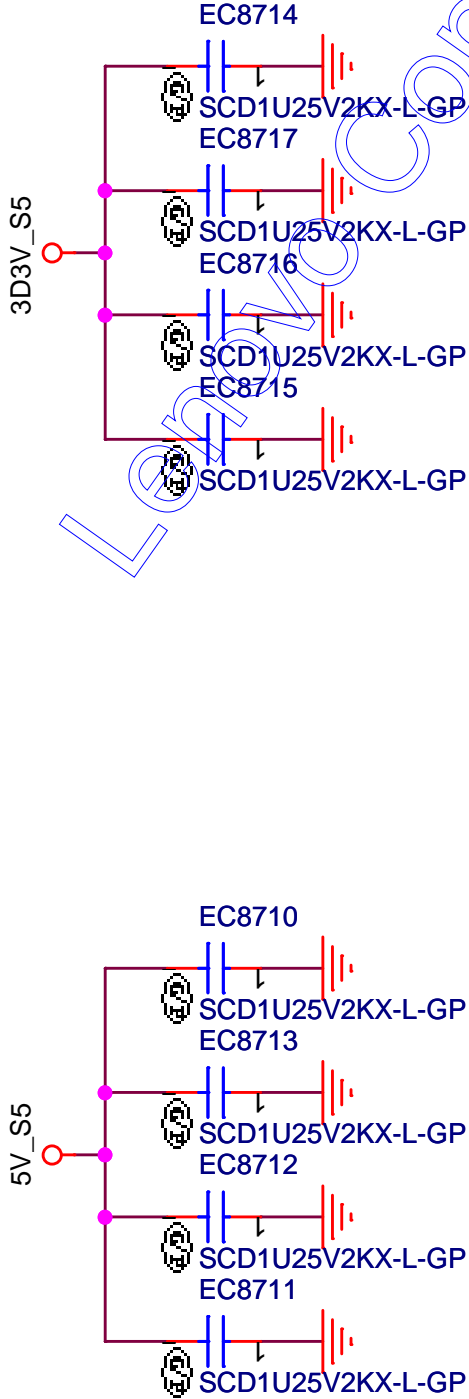
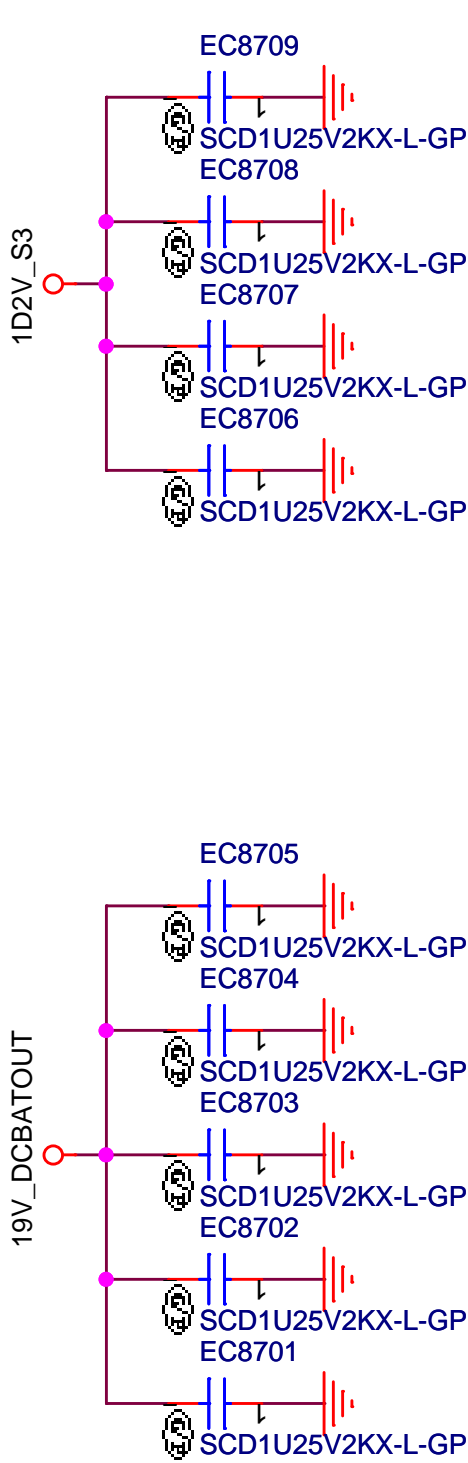


SYW232 for DGPU_1D05V

SYW232 for 1D05V
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20150604 add EMI caps



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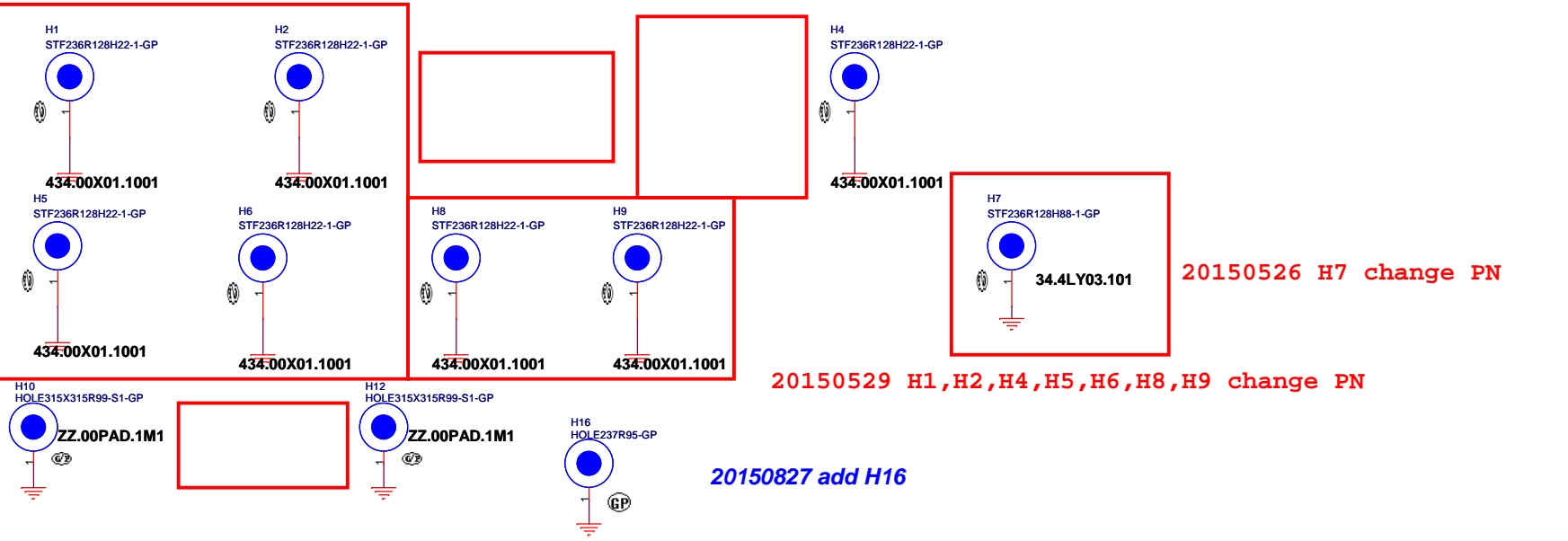
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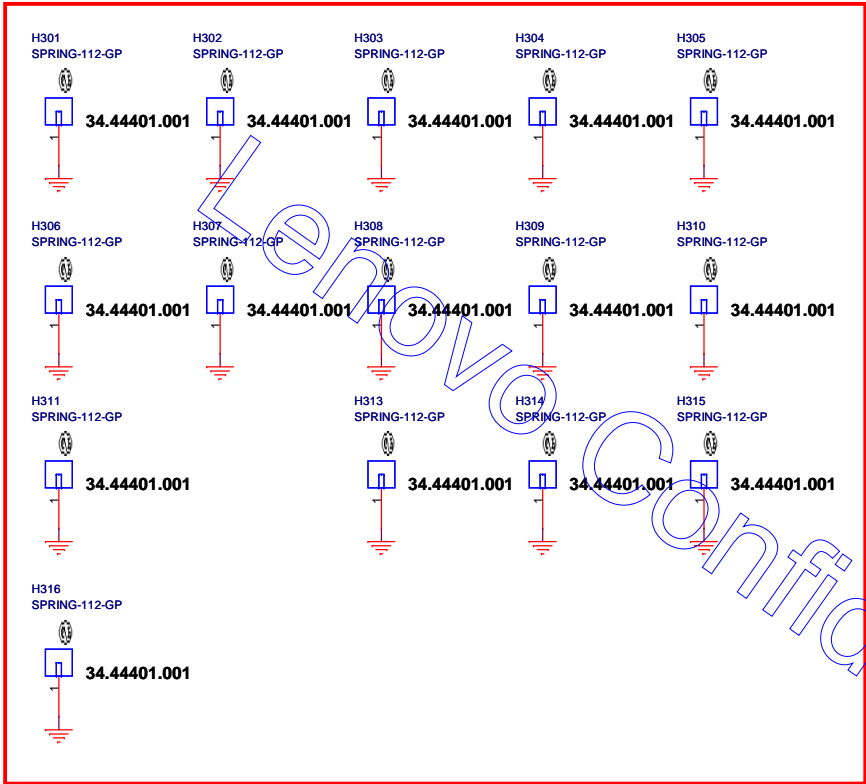
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20151007 remove H15
20150527 ME remove H3,H11
20150529 change PN



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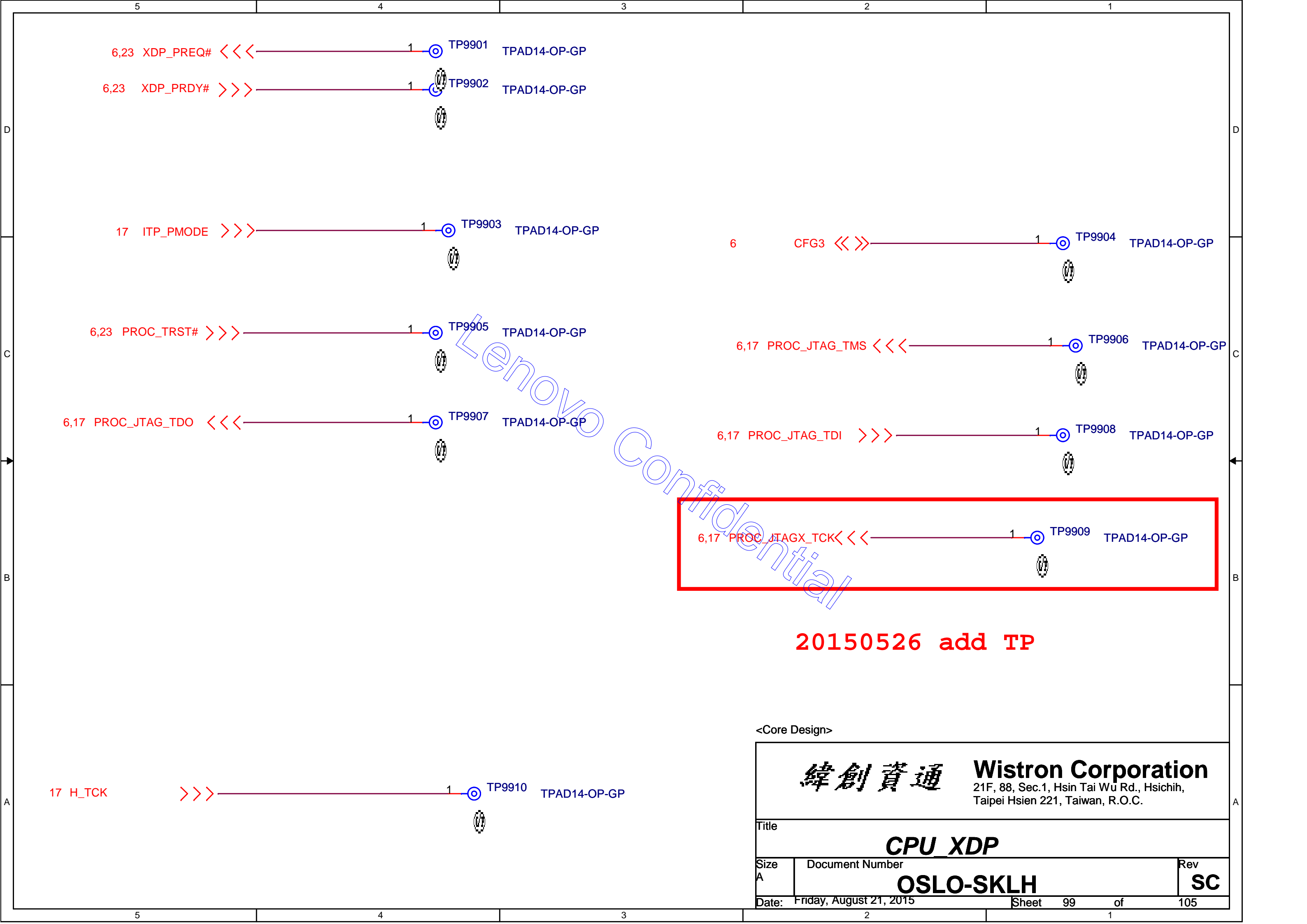
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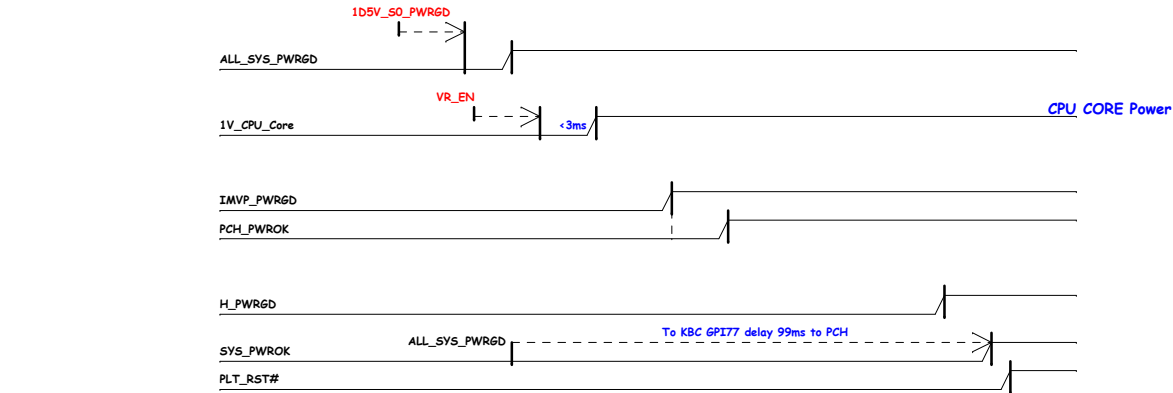
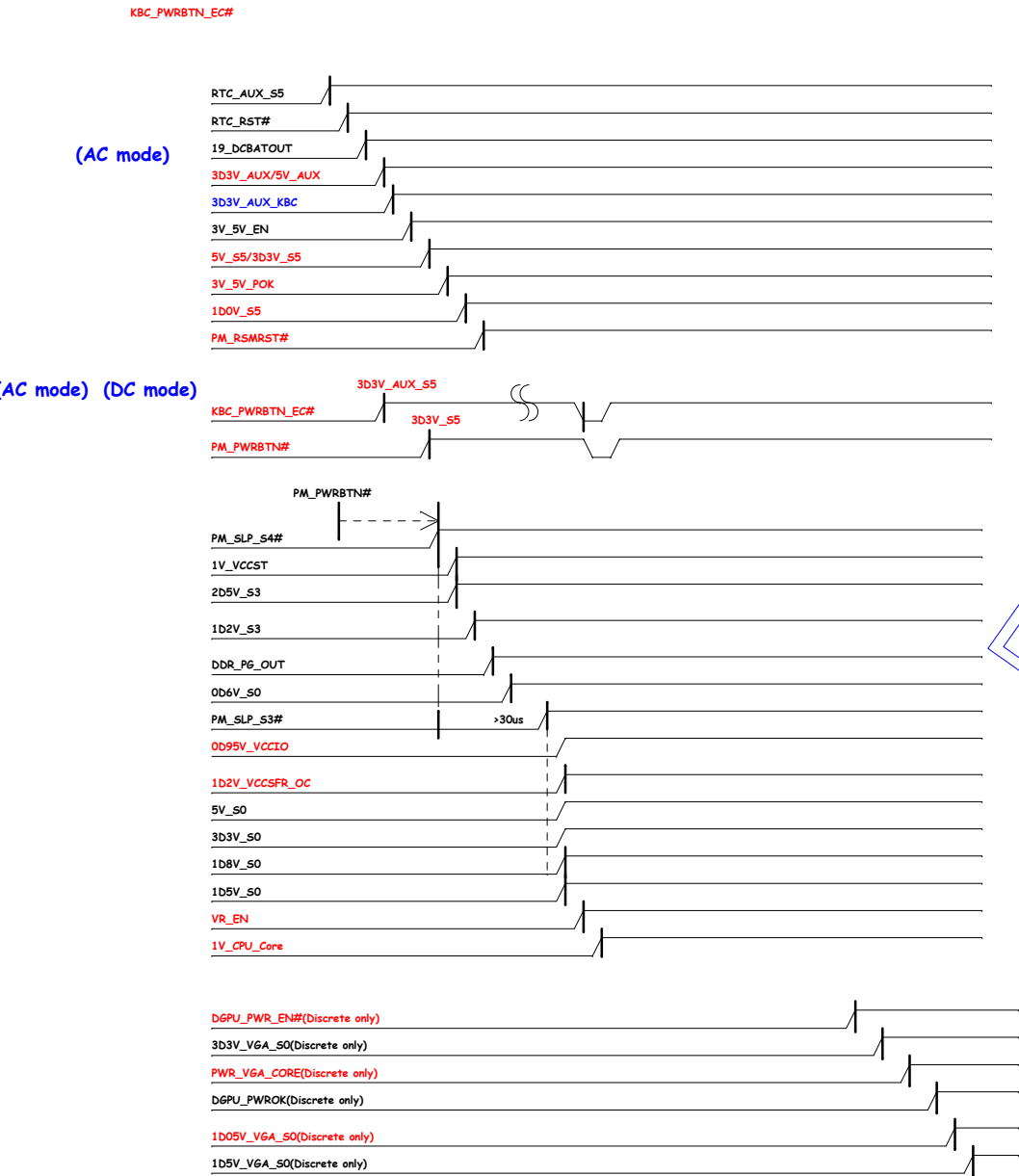
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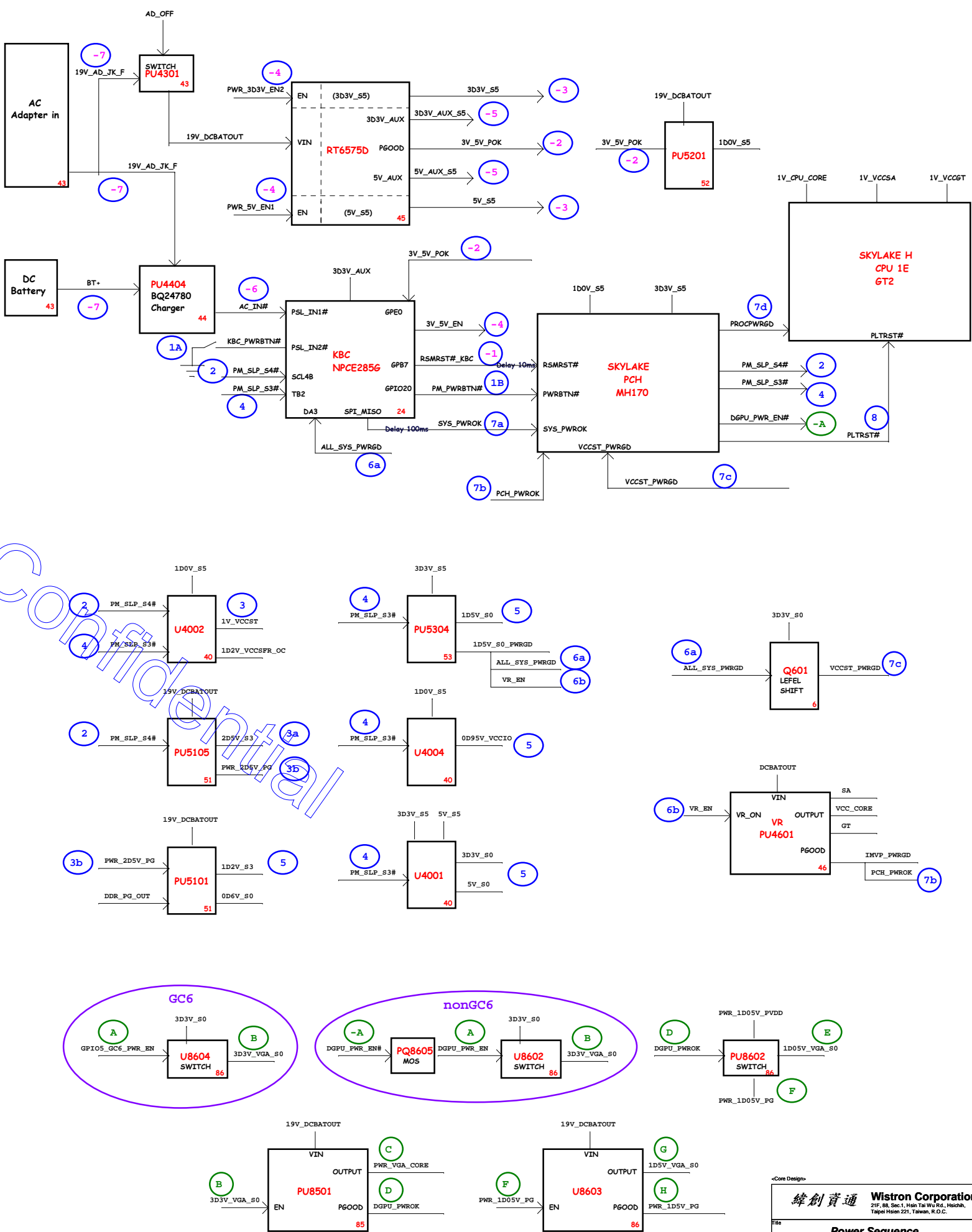
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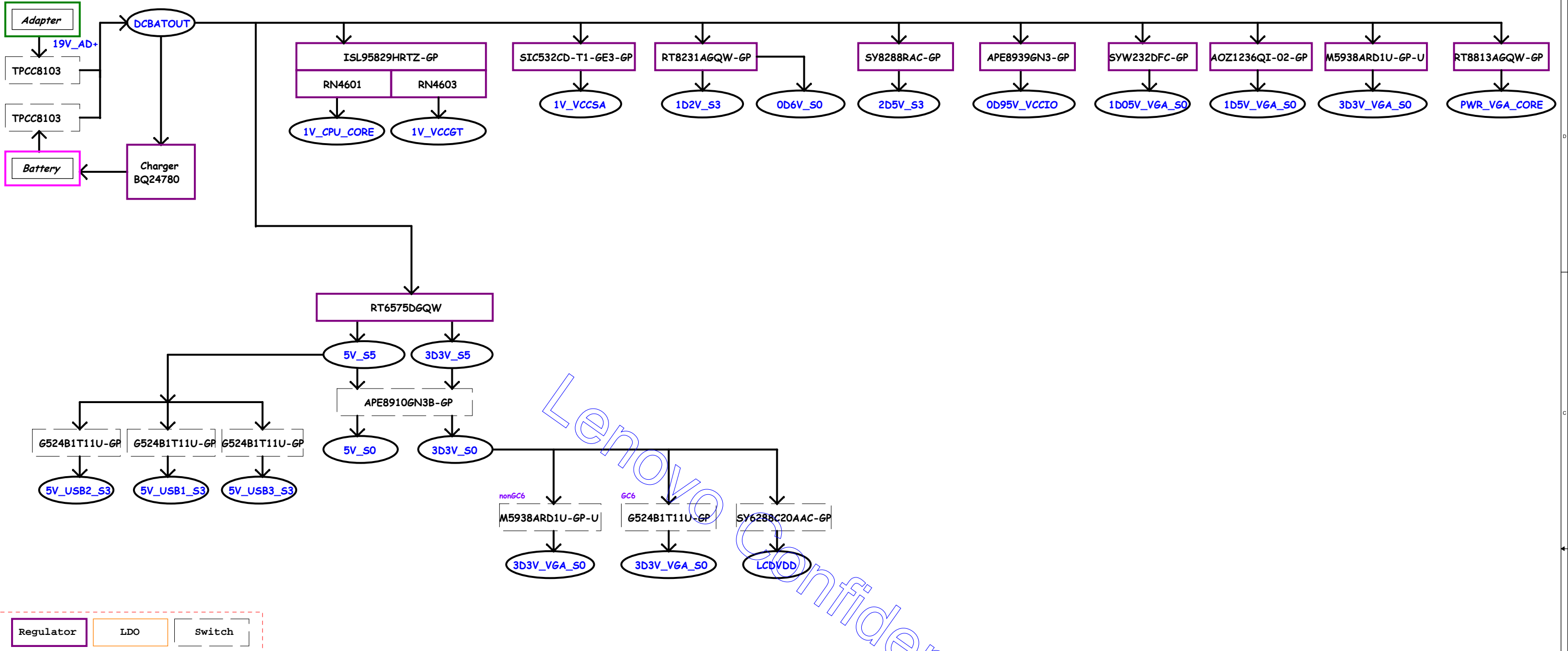
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Intel-Power Up Sequence

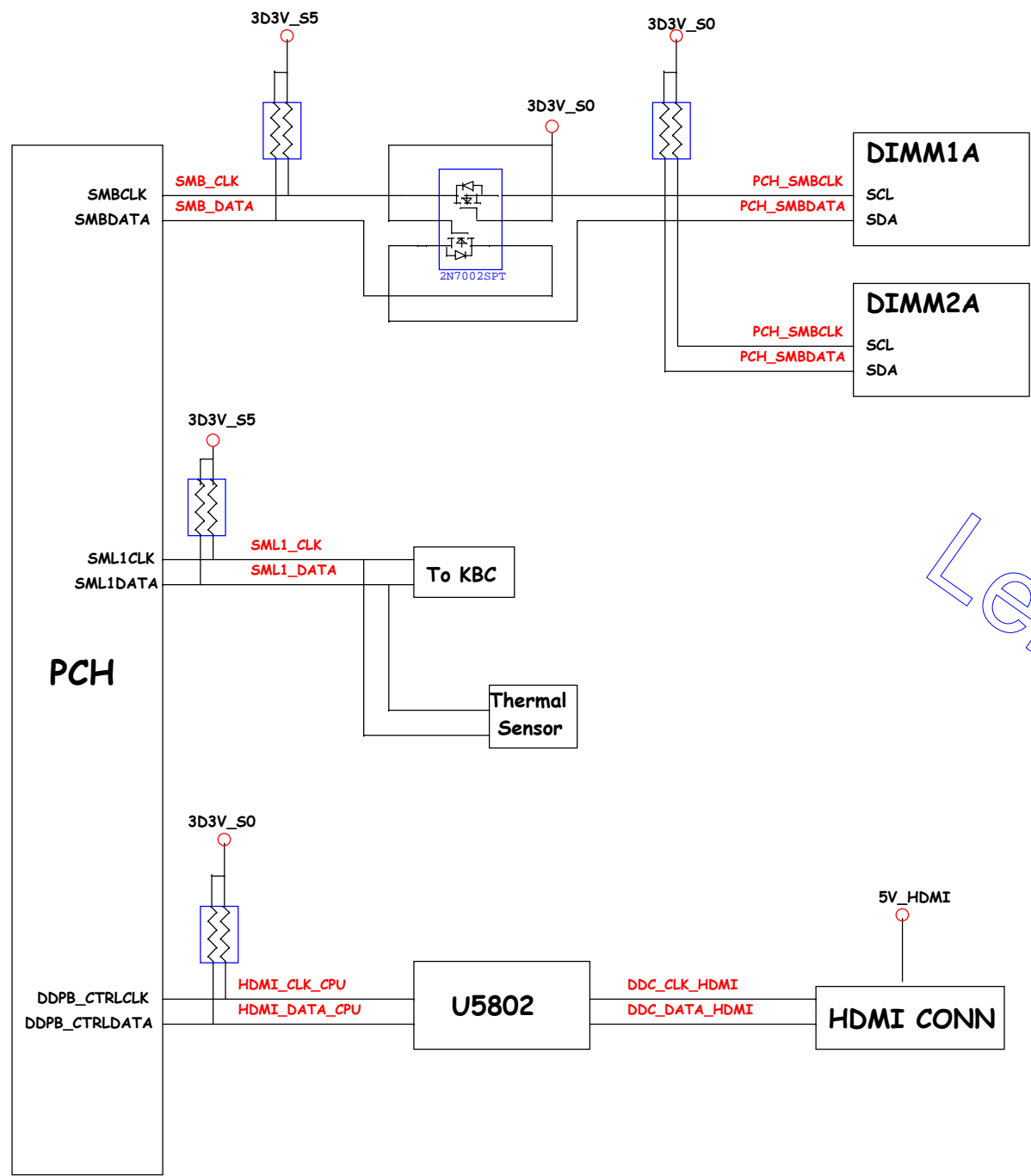


SKYLAKE H POWER UP SEQUENCE DIAGRAM

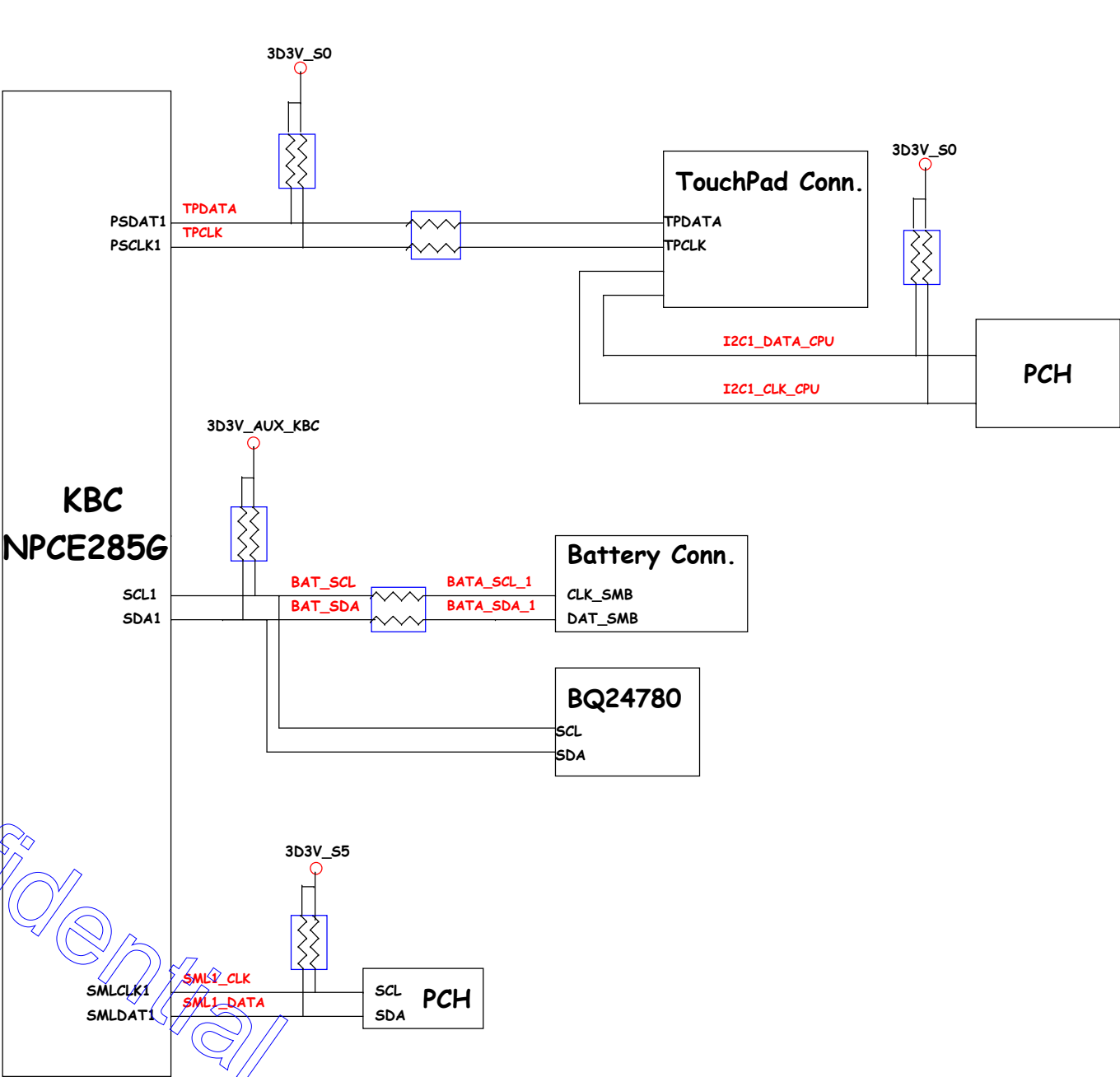




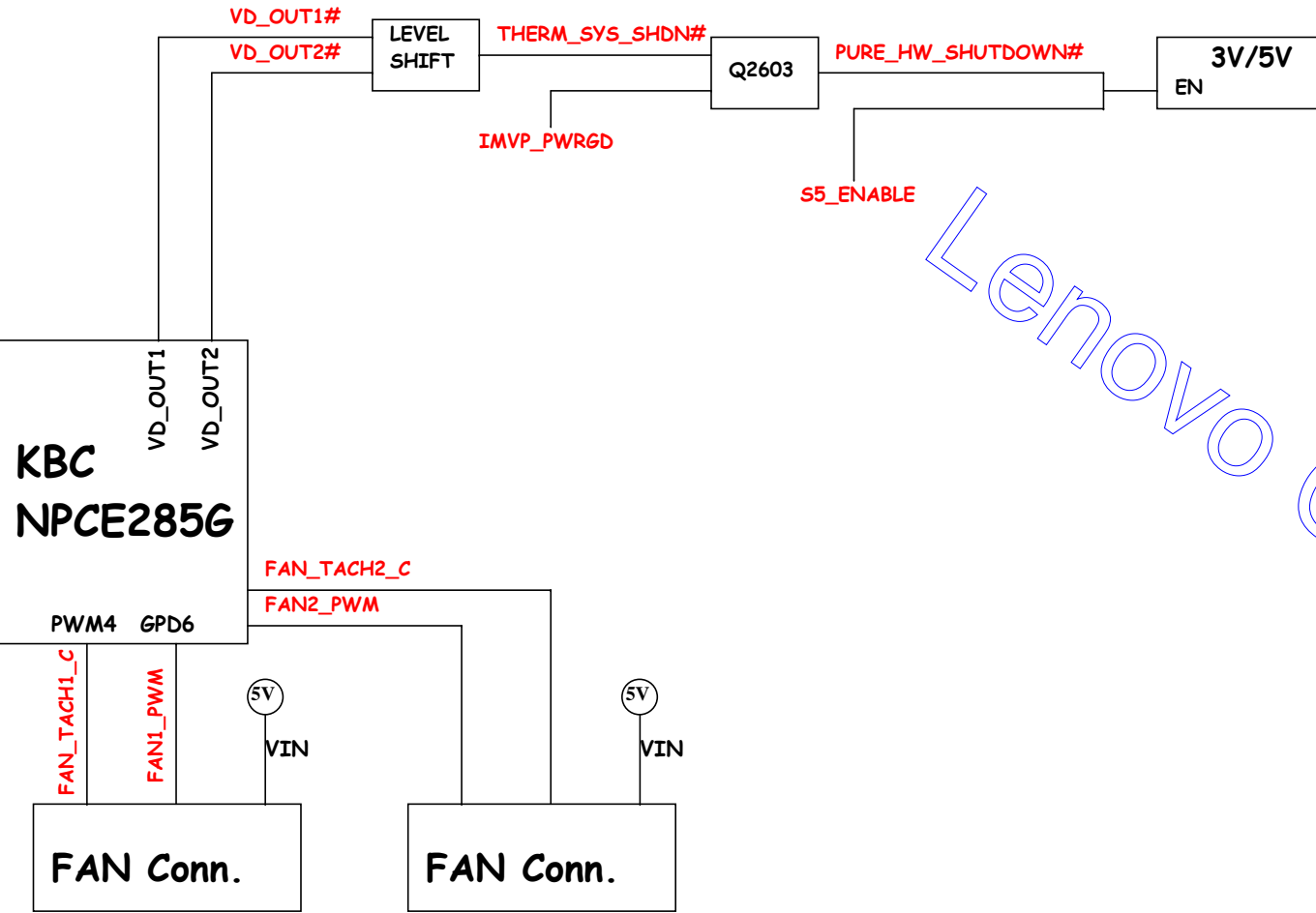
PCH SMBus Block Diagram



KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram

